OPTi Single Chip Notebook SCNB 82C463

DATA BOOK

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Disclaimer

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OPTi, Inc.

2525 Walsh Ave. Santa Clara, California 95051

Tel: (408) 980-8178
Fax: (408) 980-8860

TABLE OF CONTENTS

TABLE OF CONTENTS (con't)

TABLE OF CONTENTS (con't)

TABLE OF CONTENTS (con't)

List of Figures and Tables

1. 82C463 Overview

1.1 Introduction

The OPTi 82C463 is a highly integrated ASIC designed for high-end 32-bit portable systems. The 82C463 is a single chip solution which includes all of the AT and power management functions into one device (82C206 functions also included). The 82C463 is a superset of the proven 82C461/462 core, allowing only minimal changes made to the original BIOS. The 82C463 supports the system management modes of all new 486 CPUs. The Sequencer power management functions have been enhanced so that power management for non-SMI CPUs can be very effective. The enhanced Sequencer can now access all of the 82C463 registers and can execute conditional jumps. Its many enhanced features make the 82C463 the best choice for the expanding 32-bit portable market.

1.2 Features

1.2.1 82C463 General Features

- ❒ Supports 3.3V and 5V Intel, AMD & Cyrix SMI 486 CPUs and the "NEW" Intel Low Power 486 CPUs
- ❒ True single chip notebook implementation (internal '206) based on the proven 82C461/462 core
- ❒ Single 208-pin PQFP package implemented in 0.8u CMOS technology
- ❒ 100% IBM AT compatible solution
- ❒ Supports operation up to 33MHz at 5V and 25MHz at 3.3V
- ❒ Fully supports local bus implementations, including VESA VL-bus
- ❒ Supports Sequencer microcode, System BIOS and Video BIOS combined in a single 8-bit ROM
- ❒ Option for write protected, cacheable video and system BIOS
- ❒ Emulation of fast CPU reset and gate A20, as well as port 92h support
- ❒ Standard system requires only six TTL plus a Real Time Clock (RTC)
- ❒ Test mode support for in-circuit testing
- ❒ Two programmable chip selects and an extra software utility timer

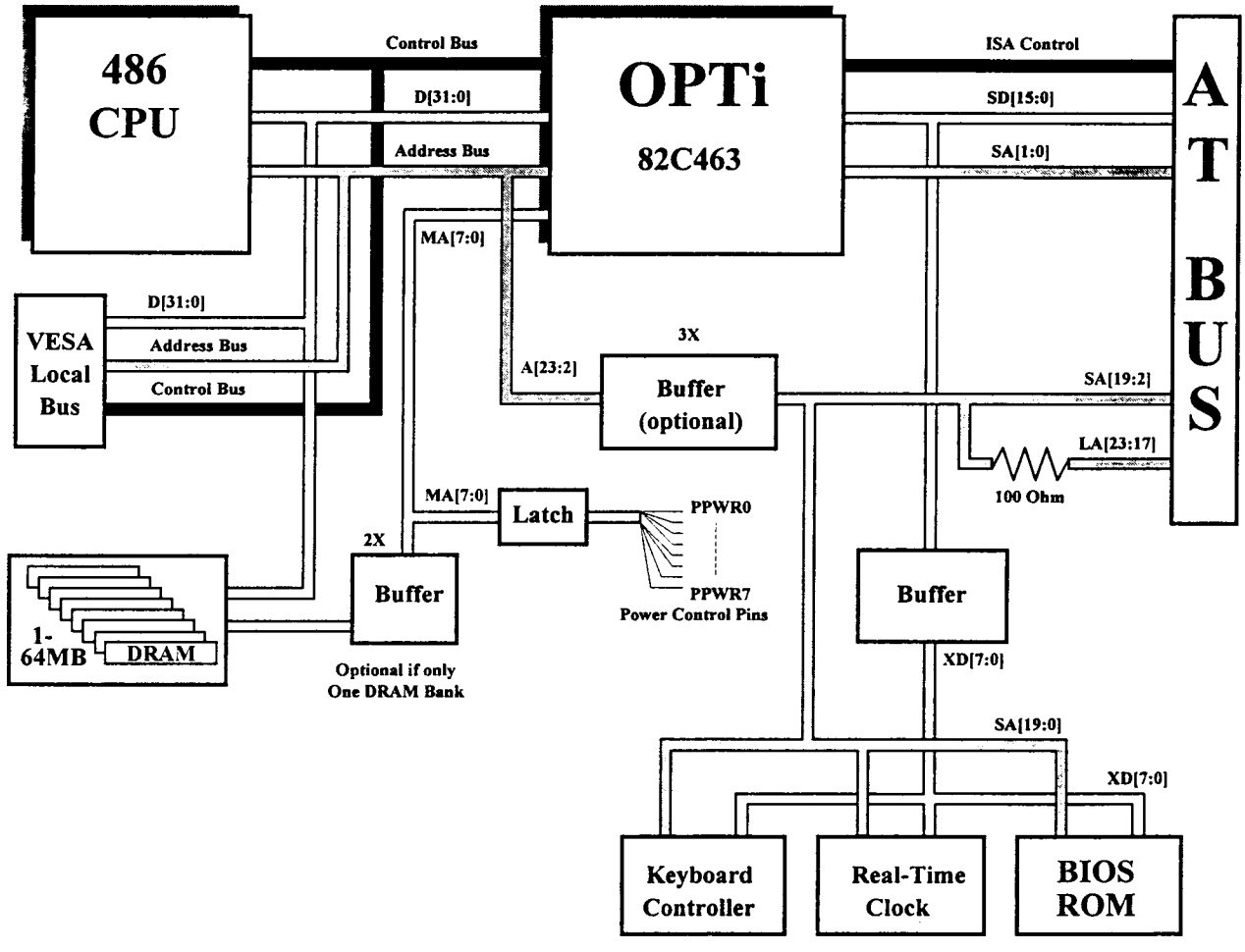
1.2.2 82C463 DRAM Controller Features

- ❒ Page-mode DRAM Controller supports 2-1-1-1, 3-1-1-1, 3-2-2-2 and 4-3-3-3 burst read memory cycles.
- ❒ DRAM controller supports zero wait state DRAM write cycles
- ❒ Supports four banks of 256K, 512K, 1M and 4M DRAMs for configurations up to 64MB
- ❒ Support for two programmable non-cacheable regions
- ❒ Fully programmable shadow RAM in C0000h-FFFFFh
- ❒ Slow refresh, CAS before RAS refresh and self-refresh support.

1.2.3 82C463 Power Management Features

- Supports SMI features of Intel, AMD & Cyrix SMI CPUs and the "NEW" Intel Low Power 486 CPUs
- Sequencer power management, with enhanced features over the 82C461/462 Sequencer
- Full Microsoft APM support, with CPU stop-clock support
- Support for CPU clock stretch function
- Supports system-level zero-volt suspend
- Flexible power saving modes with support for individual peripheral time-outs
- Operating system & application independent power management (no device drivers needed)
- 16 PMI event sources to generate SMI or to activate Sequencer
- Supports I/O trap for peripheral device power control
- Eight peripheral power control pins plus four user definable I/O pins
- RTC alarm or modem ring auto wake-up
- Suspend current leakage control
- Static AT-bus clock when AT-bus is idle.

Figure 1 : OPTi 82C463 System Block Diagram



2. 82C463 Description

2.1 82C463 Features

The OPTi 82C463 Single Chip NoteBook device (the SCNB) is a high-performance, low-power portable solution for 486 CPUs, such as the 486DLC, 486SX, 486DX and the "NEW" Intel 486 low power processors. The SCNB is a high-end "true" single chip notebook solution that contains the memory control unit [MCU], AT Bus Control Unit [BCU], the Power Management Unit [PMU], data buffers and a 82C206 type IPC (without real time clock).

The SCNB was designed with three major objectives in mind:

1) Power management without compromise on performance,
2) High efficiency design with minimum space utilization,
3) Complete compatibility and feature support.

The SCNB supports up to four banks of local memory. DRAM can be 256K, 512K, 1M or 4M for a total memory size of 64MB. Two non-cacheable areas are supported. Emulation of GATEA20 and CPURST are provided for improved performance. The 82C463 supports power management interrupts with SMI, the internal Sequencer, or a combination of both.

The Sequencer executes microcode which resides in a reserved area. If enabled, the Sequencer will take control of the system and execute the microcode to process all power management interrupts as defined by the power management registers. The mixed SMI and Sequencer power management approach can substantially improve system power savings and battery life.

2.2 System Functions

2.2.1 Reset Logic

The RST1# signal causes a "cold" reset. It is generated from the reset switch or from the power module signal representing "power good". This reset signal is used to force the system to begin execution at a known state. When RST1# is sensed active, the 82C463 asserts the CPU reset signal (CPURST) and RST4# for 128 clock cycles.

2.2.2 System Clock Generation

The SCNB provides four clocks to allow power control by controlling clock frequency. The 2X clock input OSCCLK2 is used to generate signals CLK2OUT and CPUCLK. These clocks are 2X for a 2X CPU and 1X for a 1X CPU. CLK2OUT and CPUCLK both may be divided internally using programmable divide rates to provide power control of the CPU and the SCNB. CLK2OUT is the system clock and is usually fed back into pin CLK2IN to provide the clock for most of the SCNB internal circuitry. CPUCLK is the CPU clock and may be stopped to support the stop-clock CPU function.

LCLK is used to provide a 1X clock for the local-bus when a 2X CPU is used. When a 1X CPU is used, CLK2OUT may be used for the clock to the local-bus. In this case, LCLK becomes a 2X clock that may be used for local-bus devices that require a 2X clock.

The clock input SQWIN is used to support DRAM refresh and to resume functionality during suspend. This clock input can be 32KHz or 128KHz (see Register 40h bit 3).

The OSC14 clock input is used for 82C206 functions and other miscellaneous internal uses.

The ATCLK is used for the AT bus clock. It is derived by dividing OSCCLK2 or OSC14 clock. This clock can automatically be stopped if there is no AT bus activity.

The clock output KBCLK is provided for the keyboard and KBCLK2 is KBCLK divided by two. KBCLK and KBCLK2 are used together to provide clocks for multiplexing interrupt and DMA requests.

2.2.3 Intel's "NEW" Notebook CPUs

The 82C463 supports all of the "NEW" Intel CPUs according to Intel's NDA specification.

2.2.4 Bus Arbitration Logic

The 82C463 provides arbitration between the CPU, DMA, AT bus masters and refresh logic. During DMA, AT bus master and conventional refresh cycles, the 82C463 asserts HOLD to the CPU. The CPU responds to an active HOLD signal by generating HLDA (after completing its current bus cycle) and placing most of its output and I/O pins in a high impedance state. After the CPU relinquishes the bus, the 82C463 responds by issuing RFSH# (refresh cycle) or DACK# (AT bus master or DMA cycle), depending on the requesting device.

The AT bus controller in the 82C463 arbitrates between hold and refresh requests, deciding which will own the bus once the CPU relinquishes control with the HLDA signal. The arbitration between refresh and DMA/Master is based on a FIFO priority. However, a refresh request (RFSH#) will be internally latched and serviced immediately after the DMA/Master finishes its request if queued behind HOLD. HOLD must remain active to be serviced if the refresh request comes first. DMA and bus masters share the same request pin, HOLD. The 82C463 will generate a HLDA back to the requesting device when the CPU confirms the bus free status.

2.2.5 Data Bus Conversion/Data Path Logic

The 82C463 performs data bus conversion when the CPU accesses 16 or 32-bit devices through 16 or 32-bit instructions. It also handles DMA and AT master cycles that transfer data between local DRAM or cache memory and locations on the AT bus. The 82C463 provides all the controls for the external bi-directional data buffers.

2.2.6 Numeric Co-processor Cycles (NPX)

The 82C463 monitors FERR# and NPBUSY# to provide support for the 80387 coprocessor. A coprocessor asserts FERR# during a power-on reset to indicate its presence. The coprocessor asserts NPBUSY# while executing a floating-point calculation and asserts RDYI# to the 82C463 when it is finished. If NPBUSY# is active and a co-processor error occurs (co-processor asserts FERR#), the 82C463 latches NPBUSY# and generates INT 13. Latched BUSY# and INT 13 can be cleared by an I/O port F0h write command. If the NPX is not installed , the 82C463 treats any access to the NPX address space as an AT cycle. With the NPX in place, CPU accesses to the NPX address space are direct, except for the re-synchronizing for RDYI# (the NPX ready signal) before sending RDY# back to the CPU.

2.2.7 Local Bus Interface

The 82C463 allows select peripheral devices to share the local bus with the CPU and the numeric co-processor. The performance of these devices (which may include the video sub-system, hard disk adapters, LAN and other PC / AT controllers) will dramatically increase when allowed to operate in this high speed environment. These devices are responsible for their own address and bus cycle decoding and must operate properly at the elevated frequencies required for the local CPU bus. The LDEV# input signal to the 82C463 indicates that a local-bus device will be responding to the current cycle. If this signal is sampled active at the end of the first T2 clock cycle, the 82C463 will allow the responding device to assume responsibility for the current local cycle. When the device has completed its operation, it must terminate the cycle by asserting the RDYI# pin of the 82C463. The RDYI# signal is synchronized by the 82C463 before being sent to the CPU via the RDY# line.

2.2.8 Fast GATEA20 and RESET Emulation

The 82C463 will intercept commands to port 60h and 64h so that it may emulate the keyboard controller, allowing the generation of the fast GATEA20 and fast CPURST signals. The decode sequence is software transparent and requires no BIOS modifications to function. The fast GATEA20 generation sequence involves writing "D1h" to port 64h, followed by writing "02h" to port 60h. The fast CPU "warm reset" function is generated when a port 64h write cycle with data "FEh" is decoded.

A write to port 64h with data D0h will enable the status of GATEA20 (bit 1 of port 60h) and the system reset (bit 0 of port 60h) to be readable.

Commands to system Port 92h system control Port A bits 1 (GateA20) and 0 (Fast CPU Reset) are also intercepted to provide compatibility with the PS/2. For additional information, please refer to the port descriptions in Section 5.

2.2.9 Integrated Peripheral Control Unit

The integrated peripheral control unit includes two 8237 DMA controllers, two 8259 interrupt controllers, one 8254 timer/counter and one 74612 memory mapper. It is fully compatible with the 82C206 unit.

2.3 Power Management Modes

2.3.1 Introduction

The 82C463 provides four chip level power saving modes plus flexible user definable system peripheral power saving modes. Traditional power management uses only **one** system activity detector to change between modes determined by several timers. For example, when the system detector detects no system activity and the sleep timer times out, the system will go to sleep-mode from the on-mode. After another period of time when the suspend timer times out, the system will go to suspend-mode from sleep-mode. This approach has one drawback, in that the system detector normally monitors system activities as a whole (video, FDD/HDD, keyboard, etc.), which is not very efficient because activity on any one of the devices will reload the specific timer and start the count again. If the system updates the one sub-system frequently while other sub-systems have no activity, then additional power savings could be possible to cut power to the non-active sub-systems while maintaining power to the active sub-systems. The 82C463 PMU resolves this problem by generating separate time-out PMI events for each of the major sub-systems and controlling power to these sub-systems individually. For example: Video time-out will generate PMI event #8, video next access will generate PMI event #12, disk time-out will generate PMI event #9, disk next access will generate PMI event #13, etc.. Therefore, each sub-system time-out event can turn off that sub-system's power to minimize power consumption even further.

With these individual sub-system power saving modes and chip level power saving modes, the system can easily save an additional 10% over other conventional power conservation methods.

2.3.2 Chip Level Power Management Modes

2.3.2.1 On-Mode

The on-mode indicates normal operation with all clocks running at full speed and all peripheral devices are powered up.

The 82C463 enters the On-mode under three conditions :

a) Power-on reset
b) From Standby-mode if Resume/Doze activity is detected
c) From Suspend-mode if Resume/Suspend activity is detected

2.3.2.2 Doze-Mode

The doze-mode is an intermediate power management mode and operates transparent to the user and system BIOS (does not start the Sequencer or generate SMI). When the doze-mode is enabled and one of the conditions below is met, the CPU clock speed will be reduced (selected from doze-mode speed control Register Index 41h[4:3]) or stopped. Most of the 82C463 internal circuitry will also be running at the slower speed.

The 82C463 enters this mode under two conditions:

a) The doze-timer times out
b) The APM doze command is executed

2.3.2.3 Standby-Mode

The standby-mode is used to control power to the individual subsystems and further control the CPU and system speed. The 82C463 enters this mode when a peripheral sub-system activity timer times out and PMI is generated, which will activate the Sequencer or generate an SMI.

2.3.2.4 Suspend-Mode

The suspend-mode is the deepest level of power conservation. The SMI or Sequencer routine is invoked to save the current state of the system for complete restoration at some later time. In this mode, most system power can be shut down while still retaining restorability. The 82C463 will either slow down the clock for a dynamic CPU or stop the clock for a static CPU. The leakage control function is also invoked by floating, grounding, or pulling-down all critical interface nodes to reduce the power consumption to a bare minimum.

The 82C463 enters this mode under two conditions :

a) The signal SUSP/RSM pulses (when not in suspend-mode already).
b) The appropriate internal register bit is set

2.3.3 Microsoft Windows APM Support

The 82C463 fully supports the APM power management mechanism. For total power management mode control, both the SMI and the Sequencer have access to all register bits to control power management features such as the CPU stop-clock. This makes the 82C463 flexible enough to process all commands from APM and send status back to APM.

2.3.4 CPU Clock Stretching

The majority of power consumption in CMOS circuits is due to the continuous charging of distributed capacitance by the clock signals. The 82C463 can stretch CPU write/read cycle clocks by **several** clocks each cycle (not to be confused with stretches within a clock cycle). This will reduce system power consumption significantly while still maintaining system performance, since the CPU continues to operate at maximum efficiency.

2.3.5 Sequencer Power Management

The Sequencer code resides in the EPROM area and the maximum size is 4K bytes. If the Sequencer is enabled and a PMI occurs, the 82C463 will fetch and execute the Sequencer code out of the system EPROM. The Sequencer operates much like a micro-controller. The Sequencer can do any AT bus I/O command cycle, can program and control internal registers and can execute conditional jump instructions. The CPU and the Sequencer may operate simultaneously, unless CPU executes an AT Bus cycle. In that case, the CPU must wait for the Sequencer to finish its cycle.

The Sequencer is very useful for a CPU without SMI. For this case, the Sequencer power management does not need any drivers for any operating system. A SMI CPU may use both methods (SMI and Sequencer) for even greater power management flexibility.

2.3.6 Zero-Volt Suspend

The 82C206 and the RTC have some write-only registers that can not normally be accessed. Access to these registers is vital for saving all state information to disk to support zero-volt suspend. The 82C463 solves this problem by shadowing these registers to make the register values available. This allows the whole system to be powered down during suspend. The registers in the following tables are shadowed and can be read using the Index 22h/24h scheme:

Register	PIC 1 Register	PIC 2 Register
ICW1	80h	88h
ICW2	81h	89h
ICW3	82h	8Ah
ICW4	83h	8Bh
OCW2	85h	8Dh
OCW3	86h	8Eh

Register	Index Address
Timer 1 Counter 0 Count Low byte	Register 90h
Timer 1 Counter 0 Count High byte	Register 91h
Timer 1 Counter 1 Count Low byte	Register 92h
Timer 1 Counter 1 Count High byte	Register 93h
Timer 1 Counter 2 Count Low byte	Register 94h
Timer 1 Counter 2 Count High byte	Register 95h

Write Counter H/L byte latch	Register 96h bits [5:0]
Counter Mode Register	Register 97h

RTC Index 70h	Register 98h

2.3.7 The 16 PMI Events

There are 16 PMI events which can trigger either SMI or Sequencer individually to execute power management code for that event. The following are the PMI sources :

PMI	Source
#0	LLOWBAT pin (very low battery indicator)
#1	EPMI1 pin (external PMI source)
#2	EPMI2 pin (external PMI source)
#3	LOWBAT pin
#4	IDLE_TIMER time out
#5	R_TIMER time out
#6	RESUME
#7	SUSPEND
#8	LCD_TIMER
#9	DSK_TIMER
#10	KBD_TIMER
#11	GNR_TIMER
#12	LCD_ACCESS
#13	DSK_ACCESS
#14	KBD_ACCESS
#15	GNR_ACCESS

2.3.8 The 8 Peripheral Power Pins

There are eight peripheral power pins (PPWR0-7) to control power to individual peripherals and each pin is controlled with its individual control bit in Register 54h & 55h.

The pins PPWR0 and PPWR1 have a recovery delay time associated with them when doing the suspend/resume function. These two pins could be used as a delay control for some component which needs some time to become stable once power is restored. For example, after turning off the power to the clock oscillator during suspend-mode, the resume function will restore power to the clock oscillator and wait until the clock has had time to stabilize before continuing the resume process.

During reset, the PPWRx latch signal (PPWRL) is pulsed to set the PPWRx signals to a known state. After reset PPWR[3:0] are set to 0 and PPWR[7:4] are set to 1. The PPWRx signals will remain in this state until they are updated by writing to Ports 54h and 55h.

2.3.9 Timers

There are four timers that monitor specific activity to generate PMI:

a) LCD_TIMER - Monitors video activity to generate PMI #8
b) DSK_TIMER - Monitors hard drive activity to generate PMI #9
c) KBD_TIMER - Monitors keyboard activity to generate PMI #10
d) GNR_TIMER - General purpose timer to generate PMI #11

There are two timers that monitor system activity to control doze-mode or suspend-mode :

a) DOZE_TIMER
b) IDLE_TIMER

The R_TIMER is used to generate PMI #5, but it does not monitor any pre-set activity.

The T_TIMER is used by the Sequencer.

Each timer (except the DOZE_TIMER) has four clock selections SQW[3:0]. When register 40h, bit 6 is set to 1, ALL timer clocks will be divided by an additional four (including Sequencer T_TIMER). The time intervals covered by the different selections of clock rates are shown in Table 1, Timer Rate Selections.

The DOZE_TIMER is different from the others in that it always times out after a fixed period of time. There are eight time intervals to choose from.

Table 1 : Timer Rate Selections

Additional divide by four not selected (register 40h, bit 6=0):

Choice	Clock Frequency	Time Interval Covered
SQW0 :	**32.768 KHz**	30.5us to 7.81ms
SQW1 :	**512 Hz** (8.192KHz /16)	1.95ms to 0.5 sec
SQW2 :	**16 Hz** (128 Hz /8)	62.5ms to 16 sec
SQW3 :	**0.5 Hz** (4 Hz /8)	2 sec to 512 sec (8.5 minutes)

Additional divide by four selected (register 40h, bit 6=1):

Choice	Clock Frequency	Time Interval Covered
SQW0 :	**8.192 KHz**	0.122ms to 31.25ms
SQW1 :	**128 Hz** (8.192KHz /64)	7.8ms to 2 sec
SQW2 :	**4 Hz** (128 Hz /32)	0.25 sec to 64 sec
SQW3 :	**0.125 Hz** (4 Hz /32)	8 sec to 2048 sec (34 minutes)

Important note: The additional divide-by-4 must be used with the Intel 1X-clock static CPU.

2.3.10 I/O Instruction Trap

When a timer that monitors specific activity (LCD_TIMER, DSK_TIMER, KBD_TIMER and GNR_TIMER) times out, the SMI (or the Sequencer) can be activated to turn power off to that individual device. To return power to that device, the 82C463 traps any I/O access to that device and generates SMI (or activates the Sequencer) again. This SMI (or the Sequencer) will execute code that will turn the power back on to that device.

2.3.11 AT Bus Static Mode

If this feature is enabled, the 82C463 will stretch the AT clock when there is no AT bus activity. This further reduces power consumption of peripheral devices.

2.3.12 Sequencer Description

The 82C463 can be set to respond to a Power Management Interrupt (PMI) with the internal Sequencer. The Sequencer is used to perform power management functions when SMI is inefficient or not available. When a PMI occurs, the 82C463 can execute a sequence of low-level instructions which are pre-programmed in the system ROM. The operation of the Sequencer is transparent to CPU operation.

For example, consider an IDE_TIMER time-out when the Sequencer is enabled and selected for PMI9. The Sequencer will immediately start executing the Sequencer code. This code instructs the Sequencer to turn off the IDE drive power, or send a command to the IDE to request it to go into standby-mode. After the Sequencer is done, CPU operation will continue as before. The next time the CPU accesses the IDE, the 82C463 will stop the CPU and start the Sequencer again, which turns on IDE power or sends a command to tell the IDE to return to normal operation. The CPU then continues its normal operation.

The Sequencer code is arranged in 16-byte blocks with a maximum of 256 blocks available. Each block is organized as follows:

Byte	Code
0	S
1	C1
2	C2
3	C3
4	T
5	S
6	C1
7	C2

Byte	Code
8	C3
9	T
A	S
B	C1
C	C2
D	C3
E	T
F	OPCODE

OPCODE:	bit (7:0)	'00H' means this is the last block, any number other than '00H' will be used as A(11:4) and continues to that block.

S (Set):	bits (7:6)	Selects one of four clock sources for T_TIMER. There are four clocks to choose from: SQW0, SQW1, SQW2, SQW3. See Table 1 for choices of timing intervals. Important note: The load value for this timer should not be less than five.
	bit (5)	'0' selects internal register access, '1' selects AT-bus I/O access
	bit (4:0)	Reserved

C (Command) : C1	bit (7:4)	Command select : **7 6 5 4 command** 0 1 1 0 write from C3 0 1 1 1 write from TMP(3:0) AND with C3 0 1 0 1 write from TMP(3:0), OR with C3 0 1 0 0 write from TMP(3:0), toggle bit set by C3 1 0 1 0 compare C3 and READ 1 0 1 1 compare TMP0 and TMP1, bit set by C3 1 0 0 1 compare TMP0 and READ, bit set by C3 1 0 0 0 read save to TMP(3:0) 1 1 1 0 JNE, jump not equal 1 1 1 1 JE, jump equal 1 1 0 1 JMP, jump always 1 1 0 0 stop 0 0 X X reserved
C1	bit (3:2)	Select TMP(3:0) **3 4 TMP** 0 0 TMP0 0 1 TMP1 1 0 TMP2 1 1 TMP3
C1	bit (1:0)	I/O address A(9:8) (don't cares for register access)

Sequencer code block organization (con't):

C2	bit (7:0)	I/O address A(7:0) or register index

C3	bit (7:0)	Data or mask bits D(7:0)

T (T_TIMER)	bit (7:0)	Load with T_TIMER initial count. The count rate is determined by frequency selected by the S code.

Notes :

1. Write from TMP, it will 'AND', 'OR', 'toggle' with the byte in C3, this allows modification of any bit or read-modify-write
2. Compare TMP, it only compares the bits set by C3, if C3 is '17h', it only compares bit 4 and bit (2:0)
3. For jump command, C2 defines the destination block A(11:4) and C3 defines A(3:0), C3 should be 00h, 05h or 0Ah, any other number may cause system fail.
4. Try to do move C3 to TMP, can use write from C3 to index 22h/24h
5. Try to do move TMP to TMP, can use write from TMP to index 22h/24h

2.4 DRAM Operation

During DRAM read or write cycles, a row address and a column address is required. In most DRAMs, the row address access time is longer than the column address access time. Therefore, bus performance can be improved by using page-mode DRAM operation. Memory locations sharing the same row address are on the same page, therefore, only a new column address is required. In page-mode operation, the row address strobe, RAS# can be kept active and only a new CAS# needs to be generated, thus reducing memory cycle time. In a four bank configuration, a maximum of four pages of memory can be kept active at the same time, since each bank has an independent RAS#. The effectiveness of page-mode operation depends heavily on the page size. A larger page size increases the chances of a page hit.

2.4.1 Shadow RAM

Since accesses to local DRAM are much faster than those to the EPROM, the SCNB provides shadow RAM capability. With this feature, code from slow devices like EPROM memory will be copied to local DRAM for faster access. All accesses to the specified EPROM space are redirected to the corresponding DRAM location. Shadow RAM addresses range from C0000h to FFFFFh. There is 16K granularity provided for the address range C0000h to EFFFFh, while the 64K, range from F0000h-FFFFFh (the location of the system BIOS) can be shadowed as an entire segment. The shadow RAM control is set up in the configuration registers. First, the ROM contents must be copied into the shadow RAM area. Next, the shadow RAM enable bit is set in the configuration register. For the system BIOS area, once the bit is set, the RAM area becomes read only. For the video and adapter BIOS area, the user can select read only or read/write by setting the write protect bit in the index register 32h accordingly. Video BIOS at the C0000h-C8000h area can be shadowed and cached if bit 0 of index register 35h is set to 0.

2.4.2 DRAM Configuration and MA Mapping

The SCNB supports up to 4 banks of page-mode local memory for configurations up to 64MB. 256K, 512K, 1M, or 4M page-mode DRAM devices may be used. The DRAM configuration is programmable through configuration register 34h. The DRAM performance parameters are programmable through configuration register 35h. The DRAM configurations are shown in Table 2. Note that if signal SBHE#/STRAP6 is pulled up, then pin 89 (RDYI#/CA25) takes the function of CA25, allowing memory access above 32MB to be possible. The mapping of the memory address (MA) signals is shown in Table 3.

2.4.3 DRAM Memory Re-mapping

Table 2 : DRAM Configurations

Bank 0	Bank 1	Bank 2	Bank 3	Total
256K	-	-	-	1M
256K	1M	-	-	5M
256K	1M	1M	-	9M
256K	1M	1M	1M	13M
256K	1M	4M	-	21M
256K	4M	-	-	17M
256K	4M	1M	-	21M
256K	256K	-	-	2M
256K	256K	1M	-	6M
256K	256K	1M	1M	10M
256K	256K	4M	-	18M
512K	-	-	-	2M
512K	1M	-	-	6M
512K	1M	1M	-	10M
512K	1M	1M	1M	14M
512K	1M	4M	-	22M
512K	4M	-	-	18M
512K	4M	1M	-	22M
512K	512K	-	-	4M
512K	512K	1M	-	8M
512K	512K	1M	1M	12M
512K	512K	1M	4M	24M*
512K	512K	4M	-	20M
512K	512K	4M	4M	36M*
1M	-	-	-	4M
1M	1M	-	-	8M
1M	1M	1M	-	12M
1M	1M	1M	1M	16M
1M	1M	4M	-	24M
1M	4M	-	-	20M
1M	4M	1M	-	24M
4M	-	-	-	16M
4M	1M	-	-	20M
4M	1M	1M	-	24M
4M	4M	-	-	32M
4M	4M	4M	-	48M*
4M	4M	4M	4M	64M*

* Additional DRAM configurations if signal SBHE#/STRAP6 is pulled up, enabling CA25.

Table 3 : DRAM to MA Address Mapping

Memory Address	256K		512K		1M		4M	
	Col.	Row	Col.	Row	Col.	Row	Col.	Row
MA0	A2	A11	A2	A11	A2	A11	A2	A11
MA1	A3	A12	A3	A12	A3	A12	A3	A12
MA2	A4	A13	A4	A13	A4	A13	A4	A13
MA3	A5	A14	A5	A14	A5	A14	A5	A14
MA4	A6	A15	A6	A15	A6	A15	A6	A15
MA5	A7	A16	A7	A16	A7	A16	A7	A16
MA6	A8	A17	A8	A17	A8	A17	A8	A17
MA7	A9	A18	A9	A18	A9	A18	A9	A18
MA8	A10	A19	A10	A19	A10	A19	A10	A19
MA9	---	---	---	A20	A21	A20	A21	A20
MA10	---	---	---	---	---	---	A22	A23

3. 82C463 Pinout Diagrams

3.1 OPTi 82C463 Pinout (3.3 Volts or 5 Volts only)

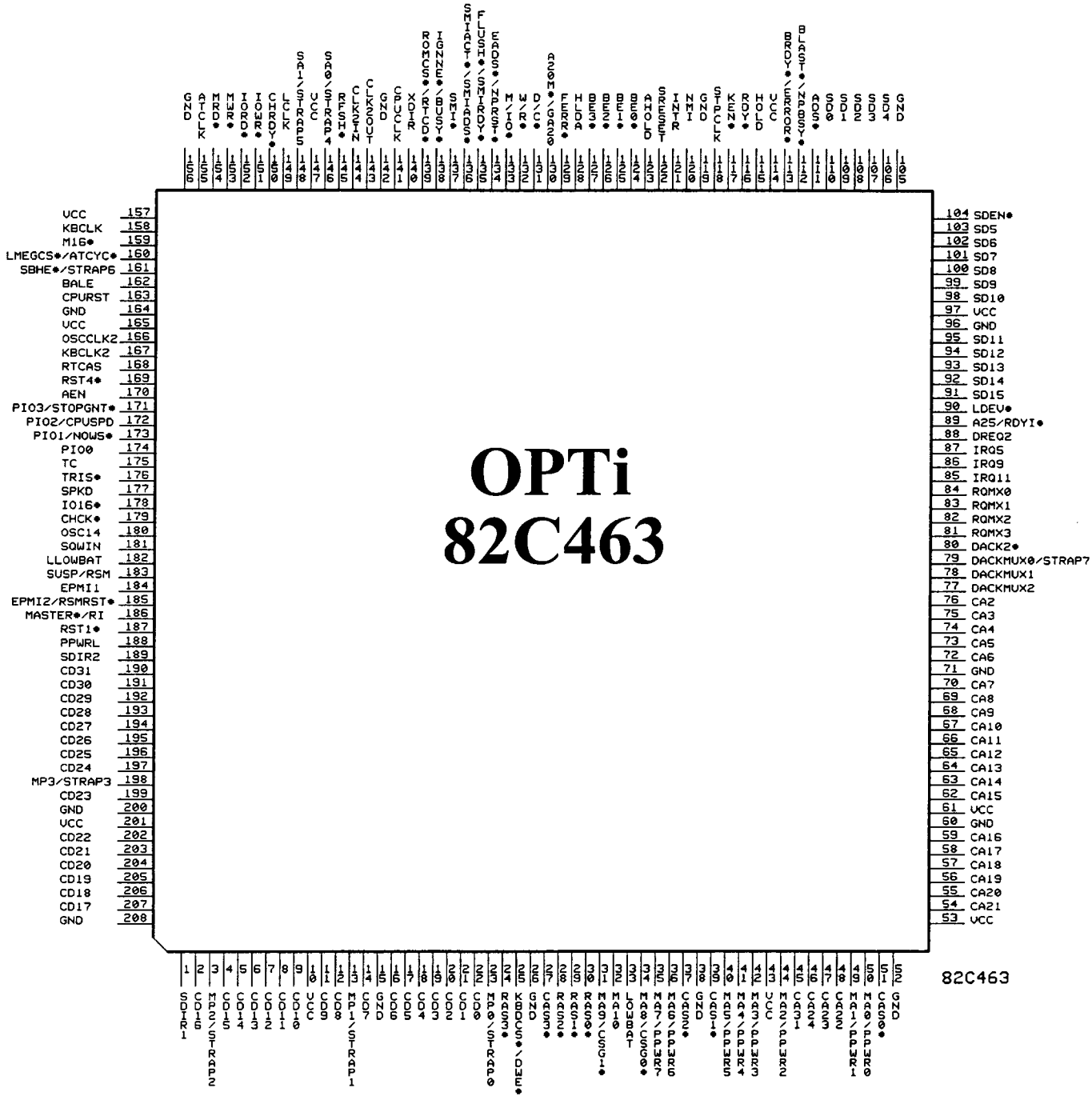


Figure 2 : OPTi 82C463 Pinout (3.3 Volts or 5 Volts only)

4. Pin Descriptions

4.1 Clock and Reset Interface

Name	Type	Pin No	Description
CLK2IN	I	144	2X clock input for 82C463 internal circuits
RST1#	I	187	Cold reset input either from power supply or reset switch
RST4#	O	169	Cold reset output
CPURST	O	163	Regular CPU reset or Intel new notebook CPU reset (includes SMBASE reset)
SRESET	O	122	CPU soft reset (for new Intel notebook CPU only)

4.2 CPU Interface

Name	Type	Pin No	Description
CD[31:0]	I/O	190-197 199,202 203-207 2,4-9,11 12,14, 16-22	CPU data bus
ADS#	I/O	111	As an input, this pin is a status from the CPU indicating a valid address cycle. As an output, this signal is used to support the VESA Local Bus
M/IO#	I/O	133	As an input, this signal comes from the CPU and indicates whether the current cycle is a Memory or I/O access. As an output, this signal is used to support the VESA Local Bus.
W/R#	I/O	132	As an input, this signal comes from the CPU and indicates whether the current cycle is a Write or Read access. As an output, this signal is used to support the VESA Local Bus.
D/C#	I/O	131	As an input, this signal comes from the CPU and indicates whether the current cycle is a Data or Code access. As an output, this signal is used to support the VESA Local Bus.
CA31	I	45	CPU address CA31 input
CA24	I	46	CPU address CA24 input
CA[23:10]	I/O	47,48, 54,55, 56-59, 62-67	CPU address lines CA23 to CA10
CA[9:2]	I/O	68-70, 72-76	CPU address lines CA9 to CA2
BE[3:0]	I/O	127-124	In CPU cycles, these signals are CPU Byte Enable [3:0]. For other cycles, they are outputs
RDY#	I/O	116	This output to the CPU indicates completion of the current bus cycle. If the RDYI#/CA25 pin is selected to be CA25 (RDYI# is not available), then a local-bus device must also drive RDY# with a tri-state driver. During a local cycle, this pin becomes an input if the RDYI#/CA25 line is selected to be CA25.

4.2 CPU Interface (con't)

Name	Type	Pin No	Description
HOLD	O	115	Hold request to the CPU to get control of the Bus
HLDA	I	128	Hold Acknowledge, This input from the CPU acknowledges a Hold Request
NMI	O	120	Non Maskable Interrupt, This output to the CPU indicates the occurrence of a Non Maskable Interrupt
INTR	O	121	Interrupt to the CPU
KEN#	O	117	This output to the 486 CPU indicates that current bus cycle is cacheable
BRDY#/ERROR#	O	113	In 486 mode: BRDY#. In 386 mode: ERROR#
EADS#/NPRST#	O	134	In 486 mode: EADS#. In 386 mode: NPRST (numeric processor reset)
AHOLD	O	123	CPU Address Hold Request, The 486 will stop driving its address bus in the clock following AHOLD going active.
BLAST# / NPBUSY#	I	112	486 mode : BLAST# indicates the next BRDY# will complete the current burst cycle. In 386 mode: NPBUSY# (numeric processor busy)

4.3 Co-Processor and Local Device Interface

Name	Type	Pin No	Description
LDEV#	I	90	Local devices may drive this input to indicate that they are responding to the current cycle. This signal must be asserted by the end of the first T2 for local device recognition.
RDYI# /CA25	I	89	The function of this pin is determined by the level on signal SBHE#/STRAP6 during reset. RDYI#: Local devices may drive this input to indicate that the current cycle is completed. CA25: Address for additional DRAM configuration. Note: This pin must function as CA25 if DRAM memory size over 32MB is required. If CA25 is used and a local device is required, the local device must drive the RDY# signal directly with a tri-state driver.
FERR#	I	129	This input is driven by the co-processor to indicate an error condition when an unmasked exception occurs
IGNNE# / BUSY#	O	138	In 486 mode, the IGNNE# output tells the CPU to ignore the numeric co-processor's error output. In 386 mode, the BUSY# is active when the co-processor is busy
LCLK	O	149	For 2X clock CPUs, this signal is the VESA local bus 1X clock. For 1X clock CPUs, this signal is the 2X clock output. (In this mode, the VESA local bus 1X clock comes from pin 143 CLK2OUT)

4.4 DRAM Interface

Name	Type	Pin No	Description
MP[3:0] / STRAP[3:0]	I/O	198,3, 13,23	DRAM parity bits. During a system reset, these pins are strapping options for CPU type selection. For pull up, use 10K resistor. For pull down, use 2.2K resistor. **Strap** **Description** **Function** MP3/STRAP3: CPU Select 1 = 486, 0 = 386 MP2/STRAP2: CPU Clock 1 = 2X clock, 0 = 1X clock Note: The status of the strap function of MP2/STRAP2 can be determined by reading Register 35h bit 3. MP[1:0] / STRAP[1:0]: **MP0 MP1 Description** 0 0 Reserved 0 1 ***AMD SMI 486:*** STPCLK is disabled and fast reset (Port 92h or 64h) generates CPURST. 1 0 ***Regular 486:*** STPCLK is disabled and fast reset (Port 92h or 64h) generates CPURST. SMIADS# is ignored (should be pulled up) 1 1 ***Intel/Cyrix SMI 486:*** STPCLK is enabled and fast reset (Port 92h or 64h) generates SRESET.
CAS[3:0]#	O	27,37, 39,51	Column Address Strobes 3 to 0. These outputs drive the CAS# inputs on DRAM bytes 3 to 0.
RAS[3:0]#	O	24,28, 29,30	Row Address Strobes 3 to 0. These outputs drive the RAS# inputs on DRAM banks 3 to 0.
MA10	O	32	Memory Address Signal MA10
MA9 / CSG1#	O	31	For DRAM cycles, this is the MA9 signal. For AT Bus cycles, this is programmable I/O chip select 1. This chip select can be used in any power management mode.
MA8 / CSG0#	O	34	For DRAM cycles, this is the MA8 signal. For AT Bus cycles, this is programmable I/O chip select 0. This chip select can be used in any power management mode.
MA[7:0] / PPWR[7:0]	O	35,36, 40,41, 42,44, 49,50	For DRAM cycles, these are MA addresses. For AT Bus cycles and Sequencer mode, these are the peripheral power control pins.

4.5 AT-Bus Interface

Name	Type	Pin No	Description
SD[15:0]	I/O	91-95, 98-103 106-110	AT Bus Data SD15 to SD0
ATCLK	O	155	AT Bus clock
BALE	O	162	AT Bus address latch
MRD#	I/O	154	AT Bus memory read command.
MWR#	I/O	153	AT Bus memory write command.
IORD#	I/O	152	AT Bus I/O read command.
IOWR#	I/O	151	AT Bus I/O write command.
CHRDY#	I/O	150	Channel ready input from AT-Bus
M16#	I/O	159	16-bit Memory Slave, AT Bus signal to indicate a 16 bit memory slave is responding. Normally an input, this signal becomes an output when a master accesses local memory
IO16#	I	178	16 bit I/O slave, AT Bus signal to indicate a 16 bit I/O slave is responding
SA[1:0] / STRAP[5:4]	I/O	148,146	AT Bus Address SA1 to SA0. They also are sampled at reset to determine the following configuration information: **SA1/STRAP5:** At reset, determines which signal will be used to generate a reset pulse for Resume sequences. Pulled-up: Selects EPMI2/RSMRST# as the reset signal for Resume operations. Pulled-down: Selects RST4# as the reset signal for Resume operations. **NOTE:** See register 40h bit 0 for additional reset control. **SA0/STRAP4:** Pulled-up: STPCLK is active low Pulled-down: STPCLK is active high
SBHE#/STRAP6	I/O	161	System Byte High Enable. Indicates a transfer on the upper byte of the AT data bus SD[15:8]. At reset, this pin determines the function of the RDYI#/CA25 pin. Pulled up: Selects pin 89 to be CA25 (In this case use RDY# for Local Device RDYI# signal). Pulled down: Selects pin 89 to be RDYI#
RFSH#	I/O	145	This is to indicate AT refresh cycles.
LMEGCS# / ATCYC#	O	160	LMEGCS# is active when the memory cycle is 0 to 1M address. It is used to generate SMRD# and SMWR#. In the AT bus I/O cycle, it is used to generate CSG0#, CSG1#.
CHCK#	I	179	AT Bus Channel Check. This signal provides the system with parity information about memory or devices on the AT bus. It indicates a non-correctable system error and is one of the sources used to generate a CPU NMI.

4.6 '206 Signals

Name	Type	Pin No	Description
RQMX3	I	81	Muxed input signals of DRQ1, DRQ3, DRQ6, DRQ7
RQMX2	I	82	Muxed input signals of IRQ10, DRQ0, IRQ12, IRQ15
RQMX1	I	83	Muxed input signals of IRQ6, IRQ8, IRQ4, DRQ5
RQMX0	I	84	Muxed input signals of IRQ3, IRQ1, IRQ7, IRQ14
IRQ11	I	85	Interrupt request channel 11
IRQ9	I	86	Interrupt request channel 9
IRQ5	I	87	Interrupt request channel 5
DREQ2	I	88	DMA request channel 2
DACKMUX0 / STRAP7	O	79	Muxed DACKx# signal, also strap pin: must be pulled high with a 10KΩ resistor.
DACKMUX[2:1]	O	77,78	Muxed DACKx# signals
DACK2#	O	80	In 486 mode it is DACK2#. In 386 mode it is NPINT for generating PREQO.
TC	O	175	AT bus Terminal count signal
AEN	O	170	AT bus address enable. This output to the AT bus indicates that the DMA controller has taken control of the CPU address bus and the AT bus command lines.

4.7 PMU Interface

Name	Type	Pin No	Description
STPCLK	O	118	STPCLK: For Intel's "NEW" notebook CPUs, it requests stop clock. The polarity of this pin is determined by the level of pin SA0/STRAP4 during res
SMI#	I/O	137	System Management Interrupt. For INTEL SMI CPU it is output only
SMIACT# / SMIADS#	I	136	Intel SMI SMIACT# or CPU with SMIADS#
FLUSH# / SMIRDY#	O	135	Intel SMI CPU FLUSH# signal or CPU with SMIRDY#
OSCCLK2	I	166	2X TTL level clock input from oscillator
CLK2OUT	O	143	System clock output. Tied to the 82C463 CLK2IN input directly. This output is 1X for 1X clock CPUs and 2X for 2X clock CPUs.
CPUCLK	O	141	CPU clock output. Tied to the 82C463 CLK2IN input directly. This output is 1X for 1X clock CPUs and 2X for 2X clock CPUs.
SQWIN	I	181	Square wave input either 32KHz or 128KHz
LOWBAT	I	33	Low battery indication (programmable polarity)
LLOWBAT	I	182	Very low battery indication (programmable polarity)
EPMI1	I	184	External user definable PMI source 1
EPMI2/ RSMRST#	I I/O	185	EPMI2 (external user definable PMI source 2) signal or the RSMRST# (Resume Reset) signal. The level during reset on the SA1/STRAP5 pin determines the function of this pin.
SUSP/RSM	I	183	Suspend/Resume function external hardware pin
TRIS#	O	176	Suspend-mode indication, '0' means 463 in suspend-mode
PIO0	I/O	174	User definable I/O pin PIO0
PIO1 / NOWS#	I/O	173	User definable I/O pin PIO1, or AT Bus Zero wait state Register 66h bit 1 will determine the function of this pin.
PIO2 / CPUSPD	I/O	172	User definable I/O pin PIO2, or CPU Full Speed indicator. 1 = full speed Register 66h bit 2 will determine the function of this pin.

4.7 PMU Interface (con't)

Name	Type	Pin No	Description
PIO3 / STPGNT#	I/O	171	User definable I/O pin PIO3 or INTEL SMI CPU stop clock grant signal Register 66h bit 3 will determine the function of this pin.
PPWRL	O	188	PPWR(7:0) Peripheral Power Control Pins latch signal. This signal is pulsed after reset to clear the PPWR(7:0) external latch.
MASTER# / RI	I	186	Modem ring indicator. Register 30h bit 5 will determine the function of this pin.

4.8 Miscellaneous Signals

Name	Type	Pin No	Description
A20M# / GA20	I/O	130	In 486 mode this pin is A20M#. In 386 mode it is GA20
RTCAS	O	168	RTC address strobe. This signal is active when the system accesses port 70h. (The Sequencer can access this port also)
SPKD	O	177	Speaker signal
ROMCS# / RTCD#	O	139	For memory cycle, this is a ROM chip select. While in the I/O cycle it is RTCD# for port 71h.
KBDCS# / DWE#	O	25	Keyboard controller chip select. The Sequencer can access the keyboard controller as well. In DRAM memory cycle, this signal is DRAM write (DWE#).
XDIR	O	140	XD bus data buffer direction control
OSC14	I	180	14.318MHz clock input
KBCLK	O	158	Keyboard controller clock
KBCLK2	O	167	Keyboard controller clock divide by 2
SDIR1	O	1	SD bus low byte direction control '1', Chip to AT Bus.
SDIR2	O	189	SD bus high byte direction control '2', Chip to AT Bus.
SDEN#	O	104	SD bus buffer enable.

4.9 Power and Ground Pins

4.9.1 Power and Ground Pins - 82C463

Name	Type	Pin No	Description
VCC	I	10,43,53,61,97,114,147,157,165,201	+5V or +3.3V
GND	I	15,26,38,52,60,71,96,105,119,142,156, 164,200,208	ground

5. Register Description

All configuration registers of the SCNB are accessed using the index/data method.
The index port is **022h** and the data port is **024h**.

5.1 Register Summary

5.1.1 Standard Registers

Index	7	6	5	4	3	2	1	0
30h (08h)	82C463 revision number		RI pin select	turbo VGA	SMI address reloc.	AT wait state	reset on halt	reserved
31h (60h)	master byte swap	reserved	parity check	dynamic SMI reloc.	ROMCS for EC000	ROMCS for E8000	ROMCS for E4000	ROMCS for E0000
32h (E4h)	select FXXXX	enable DXXXX	enable EXXXX	write protect D	write protect E	reserved	reserved	single ALE
33h (00h)	shadow EXXXX control				shadow DXXXX control			
34h (0Dh)	DRAM banks 0 & 1 configuration				reserved	DRAM banks 2 & 3 configuration		
35h (E2h)	DRAM read wait states		DRAM write wait states		1X/2X CPU	cache F (64K)	DRAM cache-able	cache C (32K)
36h (10h)	F block write	write enable C D E	write protect C	enable CXXXX	shadow CXXXX control			
37h (0Fh)	ROMCS for DC000	ROMCS for D8000	ROMCS for D4000	ROMCS for D0000	cache EXXXX control			
38h (90h)	non-cacheable block 1 (ncb1) size			ROMCS for CC000	ROMCS for C8000	ROMCS for C4000	ROMCS for C0000	ncb1 A24
39h (00h)	non-cacheable block 1 address A[23:16]							
3Ah (90h)	non-cacheable block 2 (ncb2) size			reserved				ncb2 A24
3Bh (00h)	non-cacheable block 2 address A[23:16]							
3Ch-3Fh	reserved							

5.1.2 PMU Registers

Index	7	6	5	4	3	2	1	0
40h (00h)	SMI access	timer divide select	LLOW-BAT polarity	LOW-BAT polarity	SQWIN freq. select	EPMI2 polarity	EPMI1 polarity	resume reset source
41h (00h)	DOZE_TIMER time-out select			hardware doze-mode CPU clock divide			DOZE trigger select	APM doze enable
42h (00h)	GNR_TIMER clock source		KBD_TIMER clock source		DSK_TIMER clock source		LCD_TIMER clock source	
43h (00h)	LCD monitor I/O	LCD monitor memory	LOWBAT sample rate		reserved	AT clock select		
44h (00h)	LCD_TIMER							
45h (00h)	DSK_TIMER							
46h (00h)	KBD_TIMER							
47h (00h)	GNR_TIMER							
48h (00h)	GNR_ACCESS I/O base address							
49h (00h)	GNR I/O A9	enable write	enable read	GNR_ACCESS I/O address mask				

4Ah (00h)	CSG0# base address A[8:1]				
4Bh (00)	CSG0# A9	enable write	enable read	timing select	CSG0# mask A[4:1]
4Ch (00)	CSG1# base address A[8:1]				
4Dh (00)	CSG1# A9	enable write	enable read	timing select	CSG1# mask A[4:1]

4Eh (00)	IDLE_TIMER monitor control
4Fh (00)	IDLE_TIMER

5.1.2 Register Summary (con't)

Index	7	6	5	4	3	2	1	0
50h (00h)	software start SMI	reserved	IRQ8 polarity	14.3 MHz enable	start DOZE	ready to resume	PMU mode	start suspend
51h (00h)	Sequencer base address A[17:12]						beeper control	
52h (00h)	general purpose register							
53h (00h)	general purpose register							
54h (x0h)	write mask of PPWR[3:0]				PPWR[3:0] data			
55h (xFh)	write mask of PPWR[7:4]				PPWR[7:4] data			
56h (x0h)	write mask of PIO[3:0]				PIO[3:0] data			
57h (00h)	RFSH# enable	enable INTR to PMI #6	mask FDD	mask HDD	PIO[3:0] I/O definition			

58h (00h)	LOWBAT PMI #3 configuration		EPMI2 PMI #2 configuration		EPMI1 PMI #1 configuration		LLOWBAT PMI #0 configuration	
59h (00h)	software SMI enable	resume timer reset	Resume or INTR PMI #6 and Suspend PMI #7 configuration		R_TIMER PMI #5 configuration		IDLE_TIMER PMI #4 configuration	
5Ah (00h)	GNR_TIMER PMI #11 config.		KBD_TIMER PMI #10 config.		DSK_TIMER PMI #9 config.		LCD_TIMER PMI #8 config.	
5Bh (00h)	IRQ15 select	SMI mask	Seq. enable	SMI type	enable PMI #15 & #11	enable PMI #14 & #10	enable PMI #13 & #9	enable PMI #12 & #8
5Ch (00h)	SMI source from PMI[7:0]							
5Dh (00h)	SMI source from PMI[15:8]							

5Eh (00h)	stretch mem cycle	stretch write cycle	stretch read cycle	stretch I/O cycle	stretch mem cycle	stop AT clock	AT clock stretch	reserved
5Fh (00h)	AT video load LCD timer	LB video load LCD timer	INTR resume	RI resume	number of rings			

5.1.2 Register Summary (con't)

Index	7	6	5	4	3	2	1	0
60h write	software Sequencer address A[11:4]							
61h (00h)	LOWBAT, LLOWBAT, SUSP/RSM debounce rate select				reserved	STPCLK protocol	clock switching delay	
62h (00h)	doze mode IRQ selects (see also reg. 65 bit 3)							
63h (00h)	IDLE_TIMER IRQs select							
64h (00h)	PMI #6 IRQs select							
65h (00h)	doze intr. channel	doze STPCLK active	doze sample EPMI1	recog-nize SMI	IRQ1 doze control	reserved		
66h (00h)	self refresh enable	keybd clock select	APM stop clock	suspend HOLD control	PIO3 select	PIO2 select	PIO1/ NOWS# select	STP-GNT# enable
67h (00h)	CPU type	slow refresh	PMU enable	suspend clock	reserved	CPU frequency select		
68h (00h)	R_TIMER clock source		IDLE_TIMER clock source		resume recovery time		PPWR[1:0] auto toggle	
69h (00h)	R_TIMER							
6Ah (00h)	resume IRQx select							
6Bh (00h)	Seq. ref. pulse width	SMI separate RDY	reserved			resume sources		
6Ch (00h)	TMP0							
6Dh (00h)	TMP1							
6Eh (00h)	TMP2							
6Fh (00h)	TMP3							

Notice: 1) numbers in "( )" indicate **default value**

5.2 Regular Register Description

5.2.1 Control Register 1 - Index 30h

Bit	Description	Default
[7:6]	82C463 Revision # Revision 2 is the initial production release version of the silicon	00
5	RI/MASTER# pin function (RI = modem Ring Indicator) 1 = RI, 0 = MASTER#	1
4	Turbo VGA: Enable / disable zero wait state operation at A0000h amd B0000h (NOWS# is ignored). 1 = enable, 0 = disable	0
3	Global Relocation/Translation enable for SMI addresses When using CPUs with SMI support, this bit must be set to allow relocation of SMI addresses in the 3000h segment (from the CPU) to the B000h segment and in the 4000h segment to the A000h segment in SMI memory space. 1 = enable, 0 = disable Note: Once this bit is enabled, cycle by cycle relocation is controlled by register 31h bit 4.	0
2	AT wait state control 1 = extra wait state in AT cycle, 0 = no extra wait state	0
1	Fast Reset Control (Port 92h or 64h) 1 = does not require Halt instruction 0 = requires Halt instruction before generation of CPURST (SRESET if Intel SMI)	0
0	Reserved **Important: Always write a 0 to this bit.**	0

5.2.2 Control Register 2 - Index : 31h

Bit	Description ([4-0] were previously reserved)	Default
7	Master byte swap control 1 = enable master byte swap, 0 = disable	0
6	Reserved	1
5	Parity check 1 = disable, 0 = enable	0
4	Dynamic SMI relocation The function of this bit depends on whether or not an SMI sequence is executing. **Case 1 : If no SMI sequence is running :** **1 = Allow Relocation** of addresses from the CPU in the 3000h/4000h segment to the B000h/A000h SMI memory space. This provides the mechanism for initially loading SMI code to the B000h/A000h region. **0 = Disable Relocation.** This locks out other application software from accidentally writing to the SMI memory space. The BIOS should clear this bit to 0 after loading the SMI code. **Case 2 : If SMI sequence is running :** For standard SMI sequences, the data at memory segments 3000h/4000h is not accessible by the CPU because these addresses are translated to the SMI address space at B000h/A000h. However, the following functionality has been added to allow access to this area during an SMI routine: 1 = Code fetches from the CPU in the 3000h/4000h segment will be translated from the SMI space at segment B000h/A000h (CPU D/C# = 0). Memory accesses in the 3000h/4000h space will not be translated to SMI space (CPU D/C#=1). This allows data in the 3000h/4000h memory space to be accessed and saved to disk if desired. 0 = Relocate all accesses in the 3000h/4000h segment to the B000h/A000h SMI segment. (Normal operation)	0
3	EC000h - EFFFFh Control If Register 36h bit 6 = 0: 0 = R/W from AT-Bus, 1 = R/W from ROMCS# If Register 36h bit 6 = 1: 0 = Read from AT-Bus, Write to DRAM, 1 = Read from ROMCS#, Write to DRAM.	0
2	E8000h-EBFFFh Control If Register 36h bit 6 = 0: 0 = R/W from AT-Bus, 1 = R/W from ROMCS# If Register 36h bit 6 = 1: 0 = Read from AT-Bus, Write to DRAM, 1 = Read from ROMCS#, Write to DRAM.	0
1	E4000h-E7FFFh Control If Register 36h bit 6 = 0: 0 = R/W from AT-Bus, 1 = R/W from ROMCS# If Register 36h bit 6 = 1: 0 = Read from AT-Bus, Write to DRAM, 1 = Read from ROMCS#, Write to DRAM.	0
0	E0000h-E3FFFh Control If Register 36h bit 6 = 0: 0 = R/W from AT-Bus, 1 = R/W from ROMCS# If Register 36h bit 6 = 1: 0 = Read from AT-Bus, Write to DRAM, 1 = Read from ROMCS#, Write to DRAM.	0

5.2.3 Shadow RAM Control Register I - Index : 32h

Bit	Description	Default
7	F0000h-FFFFFh control, 1 = Read from ROMCS#, write to ROMCS# (if Register 36h bit 7 = 1 or DRAM (if Register 36h bit 7 = 0) 0 = Read from DRAM and write protect	1
6	Reserved. Always write a '1'.	1
5	Reserved. Always write a '1'.	1
4	D0000h block shadow write control, 1 = write protect, 0 = writeable	0
3	E0000h block shadow write control, 1 = write protect, 0 = writeable	0
2	Reserved	1
1	Reserved (always write 0)	0
0	1 = Single ALE during bus conversion, 0 = Multiple ALE (Default)	0

5.2.4 Shadow RAM Control Register II - Index : 33h

Bit	Description	Default
7	shadow EC000h - EFFFFh, 1 = enable, 0 = disable	0
6	shadow E8000h - EBFFFh, 1 = enable, 0 = disable	0
5	shadow E4000h - E7FFFh, 1 = enable, 0 = disable	0
4	shadow E0000h - E3FFFh, 1 = enable, 0 = disable	0
3	shadow DC000h - DFFFFh, 1 = enable, 0 = disable	0
2	shadow D8000h - DBFFFh, 1 = enable, 0 = disable	0
1	shadow D4000h - D7FFFh, 1 = enable, 0 = disable	0
0	shadow D0000h - D3FFFh, 1 = enable, 0 = disable	0

5.2.5 DRAM Control Register I - Index : 34h

Bit	Description	Default
[7:4]	DRAM Bank 0 and 1 Size Configuration - Please refer to the following table	0000
3	Reserved	1
[2:0]	DRAM Bank 2 and 3 Size configuration - Please refer to the following table	111

Bits 7 6 5 4	Bank 0	Bank 1
1 0 0 0	1M	x
1 0 0 1	1M	1M
1 0 1 0	1M	4M
1 0 1 1	4M	1M
1 1 0 0	4M	x
1 1 0 1	4M	4M
1 1 1 x	x	x
0 0 0 0	256K	x
0 0 0 1	256K	256K
0 0 1 0	256K	1M
0 1 0 0	512K	x
0 1 0 1	512K	512K
0 1 1 0	512K	1M

Bits 2 1 0	Bank 2	Bank 3
0 0 0	1M	x
0 0 1	1M	1M
0 1 0	1M	4M
0 1 1	4M	4M
1 0 0	4M	x
1 0 1	x	x
1 1 0	x	x
1 1 1	x	x

5.2.6 DRAM Control Register II - Index : 35h

Bit	Description	Default
[7:6]	DRAM Read wait states 7 6 Wait States Burst Mode 0 0 0 2-1-1-1 0 1 1 3-1-1-1 1 0 1 3-2-2-2 1 1 2 4-3-3-3	11
[5:4]	DRAM Write wait states 5 4 Wait States 0 0 0 0 1 1 1 0 2 1 1 reserved	11
3	MP2/STRAP2 Status. 0 = 2x Clock, 1 = 1x Clock. This bit is read-only. A write to this bit has no effect. Note: This feature is not available on the Revision 1 Prototype Silicon.	
2	F0000h block cacheable, this bit is effective only when this block is shadowed. 0 = cacheable, 1 = non-cacheable	0
1	0 = enable DRAM cacheable range, 1 = all DRAM is not cacheable	1
0	C0000h-C7FFFh cacheable, this bit is effective only when this block is shadowed. 0 = cacheable, 1 = non-cacheable	1

5.2.7 Shadow RAM Control Register III - Index : 36h

Bit	Description	Default
7	F0000h block write control, 1 = write to ROMCS#, 0 = write to DRAM. This bit is a "don't care" if Register 32h bit 7 is set to 0	0
6	C0000h-EFFFFh Control: 0 = R/W from AT bus or ROMCS#, 1 = Read from AT-Bus or ROMCS#, always write to DRAM.	0
5	C0000h block shadow write control, 1 = write protect, 0 = writeable	0
4	Reserved. Always write a '1'.	1
3	shadow CC000h-CFFFFh, 1 = enable, 0 = disable	0
2	shadow C8000h-CBFFFh, 1 = enable, 0 = disable	0
1	shadow C4000h-C7FFFh, 1 = enable, 0 = disable	0
0	shadow C0000h-C3FFFh, 1 = enable, 0 = disable	0

5.2.8 E0000h Block Cache Enable Bits Register - Index : 37h

Bits [3:0] determine what part of the E0000 block is cacheable. These bits each controls 16Kb and are only effective when that portion of the E0000h Block has shadowing enabled (See Register 33h bits [7:4]).

Bit	Description	Default
7	DC000h-DFFFFh Control If Register 36h bit 6 = 0: 0 = R/W from AT-Bus, 1 = R/W from ROMCS# If Register 36h bit 6 = 1: 0 = Read from AT-Bus, Write to DRAM, 1 = Read from ROMCS#, Write to DRAM.	0
6	D8000h-DBFFFh Control If Register 36h bit 6 = 0: 0 = R/W from AT-Bus, 1 = R/W from ROMCS# If Register 36h bit 6 = 1: 0 = Read from AT-Bus, Write to DRAM, 1 = Read from ROMCS#, Write to DRAM.	0
5	D4000h-D7FFFh Control If Register 36h bit 6 = 0: 0 = R/W from AT-Bus, 1 = R/W from ROMCS# If Register 36h bit 6 = 1: 0 = Read from AT-Bus, Write to DRAM, 1 = Read from ROMCS#, Write to DRAM.	0
4	D0000h-D3FFFh Control If Register 36h bit 6 = 0: 0 = R/W from AT-Bus, 1 = R/W from ROMCS# If Register 36h bit 6 = 1: 0 = Read from AT-Bus, Write to DRAM, 1 = Read from ROMCS#, Write to DRAM.	0
3	EC000h to EFFFFh, 1 = non-cacheable, 0 = cacheable	1
2	E8000h to EBFFFh, 1 = non-cacheable, 0 = cacheable	1
1	E4000h to E7FFFh, 1 = non-cacheable, 0 = cacheable	1
0	E0000h to E3FFFh, 1 = non-cacheable, 0 = cacheable	1

5.2.9 Non-Cacheable Block 1 Register - Index : 38h

Non-cacheable Block 1 Index 38h - This register is used in conjunction with Index 39h to define a non-cacheable block. The starting address for the Non-Cacheable Block must have the same granularity as the block size. For example, if a 512K-byte non-cacheable block is selected, its starting address is a multiple of 512K-byte; consequently, only address bits of A19-A23 are significant, A16-A18 are "don't care".

Bit	Description	Default
[7:5]	Size of non-cacheable memory block 1: 7 5 5 Block Size 0 0 0 64K 0 0 1 128K 0 1 0 256K 0 1 1 512K 1 x x Disabled	100
4	CC000h-CFFFFh Control: If Register 36h bit 6 = 0: 0 = R/W from AT-Bus, 1 = R/W from ROMCS# If Register 36h bit 6 = 1: 0 = Read from AT-Bus, Write to DRAM, 1 = Read from ROMCS#, Write to DRAM.	0
3	C8000h-CBFFFh Control If Register 36h bit 6 = 0: 0 = R/W from AT-Bus, 1 = R/W from ROMCS# If Register 36h bit 6 = 1: 0 = Read from AT-Bus, Write to DRAM, 1 = Read from ROMCS#, Write to DRAM.	0
2	C4000h-C7FFFh Control If Register 36h bit 6 = 0: 0 = R/W from AT-Bus, 1 = R/W from ROMCS# If Register 36h bit 6 = 1: 0 = Read from AT-Bus, Write to DRAM, 1 = Read from ROMCS#, Write to DRAM.	0
1	C0000h-C3FFFh Control If Register 36h bit 6 = 0: 0 = R/W from AT-Bus, 1 = R/W from ROMCS# If Register 36h bit 6 = 1: 0 = Read from AT-Bus, Write to DRAM, 1 = Read from ROMCS#, Write to DRAM.	0
0	Address bit A24 of non-cacheable memory block 1	0

5.2.10 Non-Cacheable Block 1 Register II - Index : 39h

Bit	Description	Default
7-0	Address bit A23-A16 of non-cacheable memory block 1	0000 0000

	Valid Starting Address Bits							
Block Size	A23	A22	A21	A20	A19	A18	A17	A16
64K	V	V	V	V	V	V	V	V
128K	V	V	V	V	V	V	V	x
256K	V	V	V	V	V	V	x	x
512K	V	V	V	V	V	x	x	x

x = Don't Care
V = Valid Bit

5.2.11 Non-Cacheable Block 2 Register I - Index : 3Ah

Non-cacheable Block 2 Index 3Ah - This register is used in conjunction with Index 3Bh to define a non-cacheable block. The starting address for the Non-Cacheable Block must have the same granularity as the block size. For example, if a 512K-byte non-cacheable block is selected, its starting address is a multiple of 512K-byte; consequently, only address bits of A19-A23 are significant, A16-A18 are "don't care".

Bit	Description	Default
[7:5]	Size of non-cacheable memory block 2: 7 6 5 Block Size 0 0 0 64K 0 0 1 128K 0 1 0 256K 0 1 1 512K 1 x x Disabled	100
4	Unused	0
[3:2]	**Reserved. Always write a '1'.**	00
1	Unused	0
0	Address bits of A24 of non-cacheable memory block 2	0

5.2.12 Non-Cacheable Block 2 Register II - Index: 3Bh

Bit	Description	Default
7-0	Address bit A23-A16 of non-cacheable memory block 2	0000 0000

	Valid Starting Address Bits							
Block Size	A23	A22	A21	A20	A19	A18	A17	A16
64K	V	V	V	V	V	V	V	V
128K	V	V	V	V	V	V	V	x
256K	V	V	V	V	V	V	x	x
512K	V	V	V	V	V	x	x	x

x = Don't Care
V = Valid Bit

5.3 ROM BIOS Chip Select Register

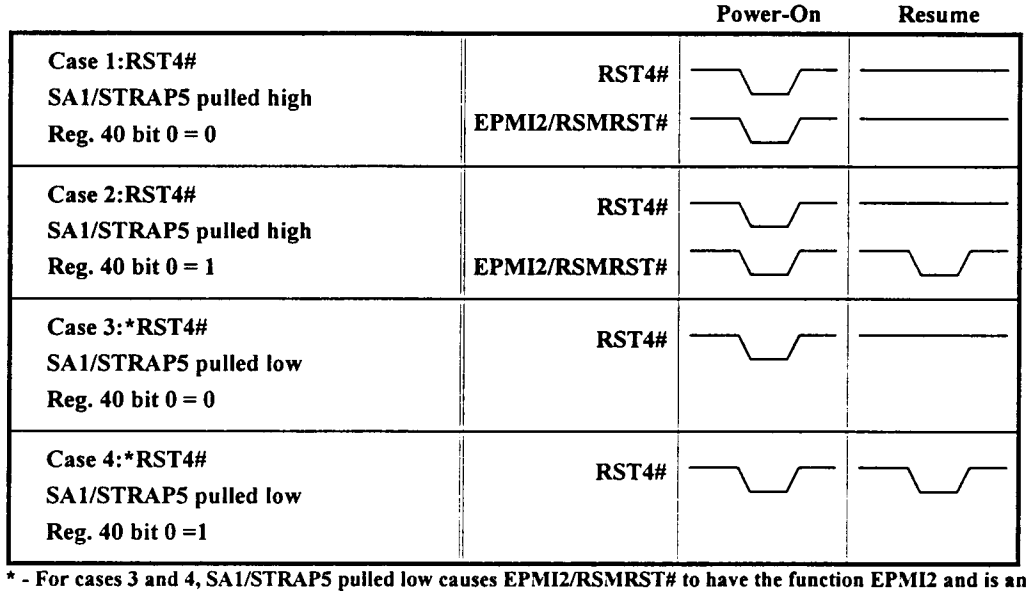
The OPTi 82C463 supports a combined system and video BIOS. The select signal ROMCS# can be set to decode the F0000h block only, the F0000h and E0000h blocks, or the F0000h, E8000h-EFFFFh and C0000h-C7FFFh blocks. The following table details how to program each of these modes.

ROMCS# Address Mode	Register 32h bit 7	Register 31h 3 2 1 0	Register 38h bit 2	Register 38h bit 1
F0000h only	1	0 0 0 0	0	0
F0000h and E0000h	1	1 1 1 1	0	0
F0000h, E8000h-EFFFFh and C0000h-C7FFFh	1	1 1 1 1	1	1

5.4 PMU Register Description

5.4.1 PMU Control Register 1 - Index : 40h

Bit	Description	Default
7	This bit is read only. 1 indicates the last read or fetch from address XXXFFFF0 was a SMIADS# cycle, 0 indicates that it is regular ADS# cycle	0
6	Global timer divide control. 0 = not divided, 1 = divided by 4. See Table 1 for the clock frequencies and timing intervals associated with each choice of this bit. **Important Note: For 1X clock Intel static CPU, this bit must be set to 1 (divide by 4 option).**	0
5	LLOWBAT polarity select , 0 = High active, 1 = Low active	0
4	LOWBAT polarity select, 0 = High active, 1 = Low active	0
3	1 = SQWIN is 128KHz, (external clock input pin), 0 = SQWIN is 32KHz	0
2	External EPMI2 pin polarity, 0 = High level active, 1 = Low level active	0
1	External EPMI1 pin polarity, 0 = High level active, 1 = Low level active	0
0	Reset source during Resume: This bit works in combination with the SA1/STRAP5 reset strapping option. It determines which signals will generate reset for resume sequences. "0" = disable (no reset pulse will be generated during resume) "1" = enable resume reset function See diagram below for description of this function.	0



*** - For cases 3 and 4, SA1/STRAP5 pulled low causes EPMI2/RSMRST# to have the function EPMI2 and is an input.**

5.4.2 PMU Control Register 2 - Index : 41h

Bit	Description	Default
[7:5]	Hardware DOZE_TIMER time-out select **7 6 5 Time Out Interval** 0 0 0 = reserved 0 0 1 = reserved 0 1 0 = reserved 0 1 1 = reserved 1 0 0 = reserved 1 0 1 = 512 ms 1 1 0 = 2 sec 1 1 1 = 8 sec	000
[4:2]	Hardware Doze-mode CPU clock select **4 3 2 CPU Doze Clock** 0 0 0 = CPUCLK / 1 * 0 0 1 = CPUCLK / 2 0 1 0 = CPUCLK / 4 0 1 1 = reserved 1 0 0 = reserved 1 0 1 = CPUCLK / 3 - Note : CPUCLK / 3 feature is not implemented in Rev.1 1 1 0 = reserved 1 1 1 = reserved *** Important Note: BIOS should use this selection when stopping the clock under APM.**	000
1	Enable LCD_ACCESS, KBD_ACCESS, DSK_ACCESS access to auto trigger the hardware DOZE_TIMER. 1 = enable, 0 = disable. When enabled, any access to these three areas will reload the hardware DOZE_TIMER. If the hardware DOZE_TIMER has timed out, any access will change CPU clock to its previous speed. Note: Please refer to Registers 43h, 57h and 5Fh for information about specific monitor areas. Please refer to Registers 44h - 46h for the LCD_ACCESS, KBD_ACCESS and DSK_ACCESS monitor areas.	0
0	APM doze-mode enable: 1 = enable APM doze-mode support, the hardware DOZE_TIMER will not function anymore, APM doze-mode is entered by writing a 1 to register 50h bit 3. 0 = disable APM doze-mode, enable hardware DOZE_TIMER	0

Note. To stop the CPU clock, the BIOS should set Register 66h bit 5 and then enter APM doze-mode via register 50h bit 3.

5.4.3 PMU Control Register 3 - Index : 42h

Bit	Description	Default
[7:6]	Clock source for GNR_TIMER. See Table 1 for the clock frequency and timing interval associated with each choice of SQWx. **7 6 clock source** 0 0 = SQW0 0 1 = SQW1 1 0 = SQW2 1 1 = SQW3	00
[5:4]	Clock source for KBD_TIMER. See Table 1 for the clock frequency and timing interval associated with each choice of SQWx. **5 4 clock source** 0 0 = SQW0 0 1 = SQW1 1 0 = SQW2 1 1 = SQW3	00
[3:2]	Clock source for DSK_TIMER. See Table 1 for the clock frequency and timing interval associated with each choice of SQWx. **3 2 clock source** 0 0 = SQW0 0 1 = SQW1 1 0 = SQW2 1 1 = SQW3	00
[1:0]	Clock source for LCD_TIMER. See Table 1 for the clock frequency and timing interval associated with each choice of SQWx. **1 0 clock source** 0 0 = SQW0 0 1 = SQW1 1 0 = SQW2 1 1 = SQW3	00

5.4.4 PMU Control Register 4 - Index : 43h

Bit	Description	Default
7	LCD_ACCESS I/O address range control, 0 = monitor I/O 3B0h - 3DFh, 1 = do not monitor I/O	0
6	LCD_ACCESS memory address range control, 0 = monitor memory A0000h-BFFFFh, 1 = do not monitor memory	0
[5:4]	LOWBAT pin sample rate, it checks the pin per sample rate. When sampled active, it generates the PMI every per sample time. If Register 40h bit 6 = 1: **5 4 Sample Time** 0 0 = 32 seconds 0 1 = 64 seconds 1 0 = 128 seconds 1 1 = reserved If Register 40h bit 6 = 0: **5 4 Sample Time** 0 0 = 8 seconds 0 1 = 16 seconds 1 0 = 32 seconds 1 1 = reserved	00
3	Reserved	0
[2:0]	AT clock select. This clock select is independent from the CPU clock select. **2 1 0 Divisor** 0 0 0 = /8 0 0 1 = /6 0 1 0 = /4 0 1 1 = /3 1 0 0 = 7.2 MHz 1 1 1 = stop All other combinations are reserved	000

The AT clock source is derived from the system clock which is divided by one of five selections : /3, /4, /6, or /8, or 7.2 MHz which is derived from the 14.318 MHz clock. The recommended divisor choice can be determined by the table below:

CPU Frequency	2x Source Frequency	/3	/4	/6	/8
12.5 MHz	25 MHz	8.1 MHz			
16 MHz	32 MHz		8 MHz		
20 MHz	40 MHz			6.6 MHz	
25 MHz	50 MHz			8.3 MHz	
33 MHz	66 MHz				8.25 MHz

5.4.5 PMU Timer Control Registers - Index : 44h, 45h, 46h, 47h, 48h and 49h

These timers are started by first performing a non-zero write to the register, followed by a dummy access within that monitor address range. When a timer times out, a PMI interrupt is generated, allowing software to turn off that device. Any subsequent access to that device will then generate another PMI interrupt to allow the software to turn that device back on.

Note: A read from registers 44h, 45h, 46h and 47h will give the initial load count only.

5.4.5.1 PMU LCD_TIMER - Index : 44h

Bit	Description	Default
[7:0]	Time count byte for LCD_TIMER. LCD_TIMER monitors LCD_ACCESS to R/W to memory address A0000h-BFFFFh or R/W to port 3B0h-3DFh. Non-zero value = time count byte for LCD_TIMER. This timer will begin to count down after a dummy access in the appropriate address range. This timer is reloaded on LCD accesses - based on mask registers 43h[7:6] and 5Fh[7:6]. **Important note: The load value for this timer should not be less than five.**	0000 0000

5.4.5.2 PMU DSK_TIMER - Index : 45h

Bit	Description	Default
[7:0]	Time count byte for DSK_TIMER. Non-zero value = time count byte for DSK_TIMER. This timer will begin to count down after a dummy access in the appropriate address range. This timer is reloaded on FDD and/or HDD accesses - based on mask register 57h [5:4]. HDD activity determined by monitoring accesses to 1F0h-1F7h and/or 3F6h. FDD activity determined by monitoring accesses to port 3F5h. A PMI is generated after this counter times out - allowing software to turn off the device. 00 = no timer count. **Important note: The load value for this timer should not be less than five.**	0000 0000

5.4.5.3 PMU KBD_TIMER - Index : 46h

Bit	Description	Default
[7:0]	Time count byte for KBD_TIMER. KBD_TIMER monitors KBD_ACCESS R/W to port 60h or 64h. Non-zero value = time count byte for KBD_TIMER. This timer will begin to count down after a dummy access in the appropriate address range. **Important note: The load value for this timer should not be less than five.**	0000 0000

5.4.5.4 PMU GNR_TIMER - Index : 47h

Bit	Description	Default
[7:0]	Time count byte for GNR_TIMER. GNR_TIMER monitors GNR_ACCESS which area is programmable. Non-zero value = time count byte for GNR_TIMER. This timer will begin to count down after a dummy access in the appropriate address range. **Important note: The load value for this timer should not be less than five.**	0000 0000

5.4.5.5 PMU GNR_ACCESS I/O Base Address - Index : 48h

Bit	Description	Default
[7:0]	GNR_ACCESS I/O base address A[8:1]. The A0 bit is always don't care.	0000 0000

5.4.5.6 PMU GNR_ACCESS I/O Function Control - Index : 49h

Bit	Description	Default
7	GNR_ACCESS I/O base address bit A9	0
6	1 = enable compare in WRITE cycle, 0 = don't compare in WRITE cycle.	0
5	1 = enable compare in READ cycle, 0 = don't compare in READ cycle.	0
[4:0]	I/O address A[5:1] mask bits. A '1' in a particular bit means that the corresponding bit in Register 48h[4:0] is not compared. This is used to decided I/O address block size.	0 0000

5.4.6 PMU Control Register - Index : 4Ah

Bit	Description	Default
[7:0]	Programmable Chip Select 0 (CSG0#) I/O base address A[8:1]. Address bit A0 is always don't care.	0000 0000

5.4.7 PMU Control Register - Index : 4Bh

Bit	Description	Default
7	Programmable Chip Select 0 (CSG0#) - I/O base address bit A9	0
6	1 = enable CSG0# for write cycles, 0 = disable.	0
5	1 = enable CSG0# for read cycles, 0 = disable.	0
4	1 = active before ALE, 0 = active just like I/O command pulse	0
[3:0]	I/O address A[4:1] mask bits. A '1' in a particular bit means that the corresponding bit in Register 4Ah[4:1] is not compared. This is used to decided I/O address block size	0000

5.4.8 PMU Control Register - Index : 4Ch

Bit	Description	Default
[7:0]	Programmable Chip Select 1 (CSG1#) I/O base address A[8:1]. Address bit A0 always don't care.	0000 0000

5.4.9 PMU Control Register - Index : 4Dh

Bit	Description	Default
7	Programmable Chip Select 1 (CSG1#) - I/O base address bit A9	0
6	1 = enable CSG1# for write cycles, 0 = disable.	0
5	1 = enable CSG1# for read cycles, 0 = disable.	0
4	1 = active before ALE, 0 = active just like I/O command pulse	0
[3:0]	I/O address A[4:1] mask bits. A '1' in a particular bit means that the corresponding bit in Register 4Ch[4:1] is not compared. This is used to decided I/O address block size	0000

5.4.10 PMU IDLE_TIMER Control Register - Index : 4Eh

The following register bits control monitor activity for these areas :

Area	I/O Address Monitored
CSG1	Defined in index 4Ah and 4Bh
CSG0	Defined in index 4Ch and 4Dh
LPT	I/O address 378h-37Fh or 278h-27Fh or 3BCh-3BFh
COM	I/O address 3F8h-3FFh or 2F8h-2FFh

Bit	Description	Default
7	IDLE_TIMER monitor CSG1, 1 = Access to the CSG1 range will reload IDLE_TIMER. 0 = Access will not reload the IDLE_TIMER	0
6	IDLE_TIMER monitor CSG0, 1 = Access to the CSG0 range will reload IDLE_TIMER. 0 = Access will not reload the IDLE_TIMER	0
5	IDLE_TIMER monitor LPT, 1 = Access to the LPT1 port area will reload IDLE_TIMER. Access is defined as Ports 378h - 37Fh, 278h - 27Fh or 3BCh - 3BFh 0 = LPT1 access will not reload the IDLE_TIMER	0
4	IDLE_TIMER monitor COM, 1 = Access to the COM port area will reload IDLE_TIMER 0 = Access will not reload the IDLE_TIMER	0
3	IDLE_TIMER monitor GNR_ACCESS area, 1 = Any access will reload IDLE_TIMER. 0 = Access will not reload the IDLE_TIMER	0
2	IDLE_TIMER monitor KBD_ACCESS area, 1 = Any access will reload IDLE_TIMER. 0 = Access will not reload the IDLE_TIMER	0
1	IDLE_TIMER monitor DSK_ACCESS area, 1 = Any access will reload IDLE_TIMER. 0 = Access will not reload the IDLE_TIMER	0
0	IDLE_TIMER monitor LCD_ACCESS area, 1 = Any access will reload IDLE_TIMER. 0 = Access will not reload the IDLE_TIMER	0

5.4.11 PMU IDLE_TIMER Control Register - Index : 4Fh

Bit	Description	Default
[7:0]	Time count for IDLE_TIMER. The IDLE_TIMER clock source select is in Register 68h [5:4]. The IDLE_TIMER time-out generates PMI #4. If the system is already in suspend-mode, then do nothing. A read from Register 4Fh will give the original loaded count only. **Important note:** The load value for this timer should not be less than five.	0000 0000

5.4.12 PMU Control Register - Index : 50h

Bit	Description	Default
7	Software starts CPU SMI writing a 1 = starts SMI writing a 0 = clears the SMI Notes: To enable this function, register 59h bit 7 must = 1 Also, the SMI routine must clear this bit otherwise it will generate an SMI request continuously.	0
6	Reserved	0
5	IRQ8 active level: 0 = Low active, 1 = High active	0
4	Turn ON/OFF internal 14.3MHz clock. This bit will turn the internal 14.3MHz clock off for power conservation. This bit does not effect KBCLK and KBCLK2. 0 = ON, 1 = OFF	0
3	Start doze-mode / read DOZE_TIMER status: This bit has two functions depending on whether it is being written to or read from: **Write:** Start APM Doze-mode 1 = start doze-mode 0 = no effect **Read:** Hardware DOZE_TIMER time-out status bit 1 = Hardware DOZE_TIMER has timed out 0 = Hardware DOZE_TIMER still counting	0
2	Ready To Resume (RTR), This bit is automatically set to 1 at the beginning of resume to indicate it is ready to perform resume program	0
1	PMU mode (READ ONLY). 1 indicates in suspend-mode. 0 means all other modes	0
0	Start Suspend: (write only; a read of this bit will always return 0). Writing a 1 to this bit will start suspend-mode. Writing a 0 will do nothing.	0

5.4.13 PMU Control Register - Index : 51h

Bit	Description	Default
[7:2]	Sequencer base address translated to A[17:12]. **Note : A19-A18 are always 1 during this operation**	0000 00
[1:0]	Beeper control (independent to port 61h) 1 0 Action 0 0 no action 0 1 1KHz 1 0 off 1 1 2KHz	00

5.4.14 PMU General Purpose Register - Index : 52h

Bit	Description	Default
[7:0]	This byte can be used as general purpose storage space	0000 0000

5.4.15 PMU General Purpose Register - Index : 53h

Bit	Description	Default
[7:0]	This byte can be used as general purpose storage space	0000 0000

5.4.16 PMU Control Register - Index : 54h

Bit	Description	Default
[7:4]	Write mask of PPWR[3:0]. 1 = enable write on corresponding bits in Register 54h[3:0]. 0 = write disable	0000
[3:0]	Read/Write data bits for PPWR[3:0]	0000

5.4.17 PMU Control Register - Index : 55h

Bit	Description	Default
[7:4]	Write mask of PPWR[7:4]. 1 = enable write on corresponding bit in Register 55h[3:0]. 0 = write disable	0000
[3:0]	Read/Write data bits for PPWR[7:4]	1111

Note : PPWR(3:0) default value is 0
PPWR(7:4) default value is 1

5.4.18 PMU Control Register - Index : 56h

Bit	Description	Default
[7:4]	Write mask of PIO[3:0]. 1 = enable write on corresponding bits in Register 56h[3:0] to PIO[3:0] port. 0 = write disable	0000
[3:0]	Read/Write data for PIO[3:0]. When these bits are read, data is latched from the pins. A write will gate data out to the pins at the end of the cycle if the direction bit is set to 1. Note : The direction of PIO[3:0] depends on the bits set in Register 57h[3:0].	0000

5.4.19 PMU Control Register - Index : 57h

Bit	Description	Default
7	Refresh Control. 1 = enable refresh, 0 = disable refresh. **Note : The BIOS needs to program this bit to 1 after power up**	0
6	PMI #6 is generated from IRQx selected in Register 64h. 1 = enable, 0 = disable.	0
5	1 = DSK_ACCESS not monitor FDD access area. 0 = DSK_ACCESS monitor FDD	0
4	1 = DSK_ACCESS not monitor HDD access area. 0 = DSK_ACCESS monitor HDD	0
[3:0]	PIO[3:0] pin direction. 1 = output, 0 = input	0000

5.4.20 PMU Event Control Registers

There are sixteen Power Management events which will trigger the PMU either to generate SMI or Sequencer individually. Following are PMI sources :

Source	Description
#0	LLOWBAT pin
#1	EPMI1 pin (External PMI source)
#2	EPMI2 pin (External PMI source)
#3	LOWBAT pin
#4	IDLE_TIMER time out
#5	R_TIMER time out
#6	RESUME (for resuming from suspend mode) or INTR (for normal mode). If it is not in suspend-mode, it is INTR when Register 57h bit 6 is set to 1 and INTR is selected by Register 64h. If it is in suspend-mode, it is RESUME which may come from SUSP/RSM pin, or INTR (selected by Register 6Ah) or RI (modem ring input). Use Register 50h bit 1 to distinguish which mode.
#7	SUSPEND
#8	LCD_TIMER
#9	DSK_TIMER
#10	KBD_TIMER
#11	GNR_TIMER
#12	LCD_ACCESS
#13	DSK_ACCESS
#14	KBD_ACCESS
#15	GNR_ACCESS

5.4.20.1 PMU Event Control Register - Index : 58h

Bit	Description	Default
[7:6]	LOWBAT PMI #3 configuration **7 6 Function** 0 0 disable 0 1 Sequencer 1 0 reserved 1 1 SMI	00
[5:4]	EPMI2 PMI #2 configuration * **5 4 Function** 0 0 disable 0 1 Sequencer 1 0 reserved 1 1 SMI	00
[3:2]	EPMI1 PMI #1 configuration * **3 2 Function** 0 0 disable 0 1 Sequencer 1 0 reserved 1 1 SMI	00
[1:0]	LLOWBAT PMI #0 configuration **1 0 Function** 0 0 disable 0 1 Sequencer 1 0 reserved 1 1 SMI	00

* Notes: EPMI1 and EPMI2 need to be asserted until recognized by its SMI service routine, since these PMIs are not latched. If EPMI1 and EPMI2 are used to place the system into suspend, the EPMIx signal must be de-asserted before the suspend instruction (Register 50h bit 0) is performed.

5.4.20.2 PMU Event Control Register - Index : 59h

Bit	Description	Default
7	Global Software SMI enable 1 = Software can start an SMI 0 = Software cannot start an SMI Note: Works in conjunction with Register 50h bit 7	0
6	Resume reset timer enables (R_TIMER, KBD_TIMER, LCD_TIMER, DSK_TIMER, GNR_TIMER, IDLE_TIMER) 1 = These timers are loaded during a resume sequence. Note: if this option is selected, any pending PMI from the timer or the access will be cleared. 0 = These timers are NOT reset during a resume sequence	0
[5:4]	Resume or INTR PMI #6 and Suspend PMI #7 configuration **5 4 Function** 0 0 disable 0 1 Sequencer 1 0 reserved 1 1 SMI	00
[3:2]	R_TIMER PMI #5 configuration **3 2 Function** 0 0 disable 0 1 Sequencer 1 0 reserved 1 1 SMI	00
[1:0]	IDLE_TIMER PMI #4 configuration **1 0 Function** 0 0 disable 0 1 Sequencer 1 0 reserved 1 1 SMI	00

5.4.20.3 PMU Event Control Register - Index : 5Ah

Bit	Description	Default
[7:6]	GNR_TIMER time out PMI #11 and access PMI #15 configuration **7 6 Function** 0 0 disable 0 1 Sequencer 1 0 reserved 1 1 SMI If 11 (or 01) is set, register 5Bh bit 3 is enabled and this timer has timed-out, then any GNR_ACCESS will generate an SMI (or start the Sequencer) immediately.	00
[5:4]	KBD_TIMER time out PMI #10 and access PMI #14 configuration **5 4 Function** 0 0 disable 0 1 Sequencer 1 0 reserved 1 1 SMI If 11 (or 01) is set, register 5Bh bit 2 is enabled and this timer has timed-out, then any KBD_ACCESS will generate an SMI (or start the Sequencer) immediately.	00
[3:2]	DSK_TIMER time out PMI #9 and access PMI #13 configuration **3 2 Function** 0 0 disable 0 1 Sequencer 1 0 reserved 1 1 SMI If 11 (or 01) is set, register 5Bh bit 1 is enabled and this timer has timed-out, then any DSK_ACCESS will generate an SMI (or start the Sequencer) immediately.	00
[1:0]	LCD_TIMER time out PMI #8 and access PMI #12 configuration **1 0 Function** 0 0 disable 0 1 Sequencer 1 0 reserved 1 1 SMI If 11 (or 01) is set, register 5Bh bit 0 is enabled and this timer has timed-out, then any LCD_ACCESS will generate an SMI (or start the Sequencer) immediately.	00

5.4.20.4 PMU Event Control Register - Index : 5Bh

Bit	Description	Default
7	IRQ15 SMI select: 0 = disable SMI select (enable IRQ15 pin function as normal) 1 = enable SMI select (SMI internally connected to IRQ15) and disable IRQ15 hardware pin function. Any PMI events generated will trigger the internal IRQ15 signal.	0
6	SMI control: 1 = mask all SMI, 0 = enable SMI	0
5	Sequencer control: 1 = enable sequence, 0 = disable all sequence	0
4	SMIACT#/SMIADS# Control: 0 = SMIACT# (Intel), 1 = SMIADS# (AMD or Cyrix)	0
3	GNR_ACCESS (Next Access) control: 1 = enable PMI source #15, 0 = disable it. Note: Disable next access PMI# here will not prevent timer PMI # from being generated.	0
2	KBD_ACCESS (Next Access) control: 1 = enable PMI source #14, 0 = disable it Note: Disable next access PMI# here will not prevent timer PMI # from being generated.	0
1	DSK_ACCESS (Next Access) control: 1 = enable PMI source #13, 0 = disable it Note: Disable next access PMI# here will not prevent timer PMI # from being generated.	0
0	LCD_ACCESS (Next Access) control: 1 = enable PMI source #12, 0 = disable it Note: Disable next access PMI# here will not prevent timer PMI # from being generated.	0

5.4.20.5 PMU SMI Source Registers - Index : 5Ch and 5Dh

For all PMIs except PMI #1 and PMI #2, Registers 5Ch and 5Dh indicate the SMI Source. When a PMI occurs, a '1' is latched into the corresponding register bit. This bit can then be read by the SMI service routine to determine which PMI generated the SMI. Writing a '1' into that particular register bit will then clear the latched PMI status. The EPMIx inputs are not latched, so if an EPMI occurs during suspend, the EPMI signal must be asserted during its SMI service routine to be recognized.

Note: Clear only one PMI source at a time.

Index : 5Ch

Bit	Description	Default
7	PMI source #7 - SUSPEND.	0
6	PMI source #6 - RESUME or INTR. *	0
5	PMI source #5 - R_TIMER time out.	0
4	PMI source #4 - IDLE_TIMER time out.	0
3	PMI source #3 - LOWBAT pin.	0
2	PMI source #2 - EPMI2 pin (External PMI source).	0
1	PMI source #1 - EPMI1 pin (External PMI source).	0
0	PMI source #0 - LLOWBAT pin.	0

* Notes: a) Clearing Register 5Ch bit 6 will clear 5Ch bit 7 also.
b) If PMI source #6 is set to Resume (Register 57h bit 6 = 0), the sources for Resume are: Modem Ring, Suspend/Resume Switch and Sources in Register 6Ah.
c) PMI #6 must be always cleared after Resume, during the Resume SMI Service Routine.

Index : 5Dh

Bit	Description	Default
7	PMI source #15 - GNR_ACCESS	0
6	PMI source #14 - KBD_ACCESS	0
5	PMI source #13 - DSK_ACCESS	0
4	PMI source #12 - LCD_ACCESS	0
3	PMI source #11 - GNR_TIMER	0
2	PMI source #10 - KBD_TIMER	0
1	PMI source #9 - DSK_TIMER	0
0	PMI source #8 - LCD_TIMER	0

5.4.20.6 PMU CPU Clock Stretch Control Register - Index : 5Eh

Bit	Description	Default
7	CPU clock stretch memory code cycle: 0 = disable, 1 = enable	0
6	CPU clock stretch write cycle: 0 = disable, 1 = enable	0
5	CPU clock stretch read cycle: 0 = disable, 1 = enable	0
4	CPU clock stretch I/O cycle: 0 = disable, 1 = enable.	0
3	CPU clock stretch memory data cycle: 0 = disable, 1 = enable	0
2	Stop ATCLK when not in AT bus cycle: 1 = enable, 0 = disable.	0
1	ATCLK stretch: 0 = asynchronous, 1 = synchronous	0
0	Reserved	0

Note: The CPU clock stretch functions are disabled when CPU clock is not /1 or /4.

5.4.20.7 PMU Control Register - Index : 5Fh

Bit	Description	Default
7	LCD_ACCESS includes AT bus video access: 0 = enable, 1 = disable	0
6	LCD_ACCESS includes Local bus video access: 0 = disable, 1 = enable	0
5	Resume Source Control. This bit controls all resume sources found in Register 6Ah. 1 = Enable resume sources, 0 = disable.	0
4	RI resume: 1 = enable, RI counter count out will generate resume. 0 = RI counter will not affect suspend status	0
[3:0]	Number of RI counts	0000

Note : Modem Ring wake up. When the RI input pin changes state and back to exceed the number set in the register, a PMI is generated to exit suspend-mode. RI should change state very slowly, minimum 240 ms high and 60 ms low.

5.5 Software Sequencer Registers

5.5.1 Software Sequencer Start Register - Index : 60h (write-only)

For Sequencer Start functions, this register is write only.

Bit	Description	Default
[7:0]	Software Invoke Sequencer Address A[11:4]. A write to Register 60h will start a Sequencer. This is one way that the CPU can generate a Sequencer event without the PMI. A write of 00h to Register 60h will do nothing. Any non-zero write to Register 60h will be used as A[11:4] to start the Sequencer.	0000 0000

5.5.2 Debounce Register - Index : 61h

For debounce functions this register is write only.

Bit	Description	Default
[7:6]	LOWBAT and LLOWBAT pin debounce rate select 7 6 Function 0 0 no debounce 0 1 0.25ms 1 0 8ms 1 1 0.5 sec	00
[5:4]	SUSP/RSM pin debounce rate select 5 4 Function 0 0 reserved 0 1 latch high to low edge 1 0 4ms (low to high) 1 1 8ms (low to high)	00
3	**Reserved. Always write '0'.**	0
2	STPCLK protocol for switching CPU clock 2X type CPUs do not need to enable protocol or stop the CPU clock when changing frequencies 1 = 1X clock type or DX2 type CPUs (enable protocol). Also enable Register 66h bit 3 and/or bit 0 (see Register 66h bits 3 and 0). 0 = 2X clock type CPUs (disable protocol)	0
[1:0]	1X clock type CPU STPCLK# delay. Note: 2X type CPUs should program "no delay" for clock switching. b1 b0 Delay 0 0 No Delay 0 1 120us 1 0 240us 1 1 1ms	00

5.5.3 IRQ DOZE Register - Index : 62h

This register selects which interrupts will be used to control doze-mode operation.
Note: When enabled, a read of this register will indicate active sources at that time.

Hardware doze-mode:	The selected interrupts will be used to re-load the hardware DOZE_TIMER and/or trigger the system out of doze-mode.
APM doze-mode:	The selected interrupts will be used to trigger the system out of doze-mode only.

Note: Please refer to Register 65h bit 3 for doze-mode IRQ1 control.

Bit	Description	Default
7	IRQ13: 1 = enable, 0 = disable.	0
6	IRQ8: 1 = enable, 0 = disable.	0
5	IRQ7: 1 = enable, 0 = disable.	0
4	Doze-mode IRQ select register. IRQ12 (PS/2 Mouse) can trigger doze-mode exit. This register selects which IRQx inputs can individually reload the DOZE_TIMER exit from the doze-mode. 1 = enable - IRQ12 trigger will force doze-mode exit 0 = disable - IRQ12 has no effect on doze-mode exit	0
3	IRQ5: 1 = enable, 0 = disable.	0
2	IRQ4: 1 = enable, 0 = disable.	0
1	IRQ3: 1 = enable, 0 = disable.	0
0	IRQ0: 1 = enable, 0 = disable.	0

5.5.4 IDLE_TIMER Select Register - Index : 63h

Bit	Description	Default
7	EPMI1: 1 = enable, 0 = disable. (level trigger)	0
6	IRQ13: 1 = enable, 0 = disable.	0
5	IRQ8: 1 = enable, 0 = disable.	0
4	IRQ7: 1 = enable, 0 = disable.	0
3	IRQ5: 1 = enable, 0 = disable.	0
2	IRQ4: 1 = enable, 0 = disable.	0
1	IRQ3: 1 = enable, 0 = disable.	0
0	IRQ0: 1 = enable, 0 = disable.	0

Note : When enabled, that IRQ active will reload IDLE_TIMER. A read of this register will indicate active sources at that time.

5.5.5 Normal PMI #6 - IRQ Select Register - Index : 64h

Bit	Description	Default
7	IRQ14: 1 = enable, 0 = disable	0
6	IRQ8: 1 = enable, 0 = disable	0
5	IRQ7: 1 = enable, 0 = disable	0
4	IRQ6: 1 = enable, 0 = disable	0
3	IRQ5: 1 = enable, 0 = disable	0
2	IRQ4: 1 = enable, 0 = disable	0
1	IRQ3: 1 = enable, 0 = disable	0
0	IRQ1: 1 = enable, 0 = disable	0

Note : When enabled, the active IRQ will generate PMI #6. A read of this register will indicate active sources at that time.

5.5.6 DOZE Register - Index : 65h

Bit	Description	Default
7	All interrupt channels (INTR signal) can be monitored during Doze mode. 1 = enable, 0 = disable	0
6	Doze mode STPCLK control (used only if register 61h bit 2 = 1) 1 = STPCLK will latch, for stopping the CPU clock (APM). Delay is determined by Register 61h bits [1:0]. 0 = STPCLK will pulse, for changing the frequency of the CPU clock. The pulse width is determined by Register 61h bits [1:0].	0
5	If enabled, the EPMI1 pin is monitored during Doze mode (32KHz sample) 1 = enable, 0 = disable	0
4	Recognize SMI during APM stop clock. 1 = enable, 0 = disable.	0
3	If enabled, IRQ1 can trigger system out of Doze mode. 1 = enable, 0 = disable Notes: a) This bit is write-only. b) This bit is used in conjunction with register 62h. c) When enabled, a read of this register will indicate active sources at that time.	0
[2:0]	Reserved	000

5.5.7 Control Register - Index : 66h

Bit	Description	Default
7	Select self refresh during suspend, 0 = normal refresh, 1 = self refresh	0
6	Select KBCLK during suspend, 0 = 7.16 MHz (14.318 MHz /2), 1 = 32 KHz	0
5	Software (APM) CPU stop-clock control If this bit is enabled, the CPU clock can be stopped by entering APM Doze mode (program Register 50h bit 3 Start Doze to 1)'. If this bit is disabled, then Register 50h bit 3 'Start Doze' will use the Hardware Doze mode clock select. 1 = enable, 0 = disable	0
4	Suspend mode Hold Select 1 = Suspend will NOT generate HOLD signal 0 = Suspend mode will generate HOLD signal	0
3	PIO3 pin select: 0 = PIO3 pin. 1 = STPGNT# input. Enable this bit if the CPU uses STPGNT# pin. Index 57h bit 3 should be set to 0 for input mode.	0
2	PIO2 pin select: 0 = PIO2 pin, 1 = CPU speed indicator output (1 = full speed, 0 = not in full speed). Note: Index 57h bit 2 must be set to 1 for PIO2 to be in output mode (to indicate CPU speed).	0
1	PIO1/NOWS# pin select. This bit determines the function of the multiplexed pin PIO1/NOWS#. Note that this selection can be made after Reset has occurred so an external strap resistor is not needed. 1 = select NOWS#, 0 = select PIO1	0
0	STPGNT# protocol enable, 0 = disable, 1 = enable. When disabled, the CPU clock can be stopped without waiting for STPGNT#. Enable this bit if the CPU generates STPGNT# cycle.	0

5.5.8 Control Register - Index : 67h

Bit	Description	Default
7	0 = Static CPU: In suspend-mode, 82C463 will stop CPU clock. 1 = Dynamic CPU: In suspend-mode, the CPU clock speed depends on register 67h bit 4 or by BIOS selecting the CPU clock by setting register 67h bits [3:0] before the start of the suspend state.	0
6	1 = slow refresh (128µs), 0 = normal refresh (15µs)	0
5	PMU global control: 1 = enable PMU, 0 = disable.	0
4	Dynamic CPU clock select during suspend. 0 = /8 for Dynamic CPU clock during suspend. **Setting this bit to 1 will not change CPU clock.** The PMI #7 service routine or Sequencer should change the CPU clock before entering suspend state.	0
3	Reserved	0
[2:0]	CPU clock frequency select **2 1 0 Frequency** 0 0 0 CPUCLK / 1 0 0 1 CPUCLK / 2 0 1 0 CPUCLK / 4 0 1 1 reserved 1 0 0 reserved 1 0 1 CPUCLK / 3 Note: this selection is not implemented in Rev. 1 (reserved). 1 1 0 reserved 1 1 1 reserved	000

5.5.9 Control Register - Index : 68h

Bit	Description	Default
[7:6]	R_TIMER clock source select. See Table 1 for the clock frequency and timing intervals associated with each choice of SQWx. 7 6 Source 0 0 SQW0 0 1 SQW1 1 0 SQW2 1 1 SQW3	00
[5:4]	IDLE_TIMER clock source select. See Table 1 for the clock frequency and timing intervals associated with each choice of SQWx. 7 6 Source 0 0 SQW0 0 1 SQW1 1 0 SQW2 1 1 SQW3	00
[3:2]	Resume recovery time. These two bits determine the recovery time from PPWR(1:0) active after a resume until the end of reset. The RSMRST# signal and/or RST4# is active during this recovery time. The clock is guaranteed to be active for at least the last 1/8 of the recovery time. These bits are not affected by Register 68h [1:0]. 3 2 Recovery Time 0 0 8ms 0 1 32ms 1 0 128ms 1 1 30us	00
[1:0]	PPWR(1:0) suspend auto toggle enable. These two pins can be set to automatically toggle when entering or exiting suspend mode. When register 68h bit 0 is set to 1 and Suspend Mode is entered, the inverse of Register 54h bit 0 will be written to the PPWR0 pin (mask bit register 54h bit 4 has no affect here). When exiting Suspend mode, Register 54h bit 0 is written to PPWR0, followed by a delay for recover time as set in Register 68h[3:2] before continuing the resume. Register 68h bit 1 acts the same with respect to the PPWR1 pin. 1 = enable, 0 = disable	00

5.5.10 R_TIMER Control Register - Index : 69h

Bit	Description	Default
[7:0]	Time count for R_TIMER. The R_TIMER starts to count after a non-zero write to this register. A read from this register gets the current count. **Important note:** The load value for this timer should not be less than five.	0000 0000

5.5.11 Resume IRQ Register - Index : 6Ah

Bit	Description	Default
7	EPMI2 trigger: A rising edge will cause 82C463 resume from suspend-mode. * 1 = enables this function, 0 = disables it	0
6	EPMI1 trigger: A rising edge will cause 82C463 resume from suspend-mode. * 1 = enables this function, 0 = disables it	0
5	IRQ8 trigger: A falling edge will cause 82C463 resume from suspend-mode. 1 = enables this function, 0 = disables it	0
4	IRQ7 trigger: A rising edge will cause 82C463 resume from suspend-mode. 1 = enables this function, 0 = disables it	0
3	IRQ5 trigger: A rising edge will cause 82C463 resume from suspend-mode. 1 = enables this function, 0 = disables it	0
2	IRQ4 trigger: A rising edge will cause 82C463 resume from suspend-mode. 1 = enables this function, 0 = disables it	0
1	IRQ3 trigger: A rising edge will cause 82C463 resume from suspend-mode. 1 = enables this function, 0 = disables it	0
0	IRQ1 trigger: A rising edge will cause 82C463 resume from suspend-mode. 1 = enables this function, 0 = disables it	0

Note : A read of this register will read active sources at time of the register read (not latched).
* An SMI will not be generated necessarily if an EPMIx is enabled here. Please see register 58h to generate SMI if that is desired.

5.5.12 Resume Source Register - Index : 6Bh

Bit	Description	Default
7	Sequencer refresh pulse width: 0 = 4 AT clocks, 1 = 6 AT clocks	0
6	1 = separate SMIRDY for SMIADS, 0 = regular RDY for SMIADS	0
[5:3]	Reserved	000
[2:0]	Resume sources, read only **2 1 0 Resume Source** 0 0 0 Keyboard IRQ 0 0 1 RI 0 1 0 INTR 0 1 1 LPT1 IRQ 1 0 0 SUSP/RSM pin 1 0 1 EPMI2 1 1 0 COM1 IRQ 1 1 1 COM2 IRQ	000

5.5.13 TMP Registers - Index : 6Ch to 6Fh

These four TMP registers can be directly accessed by the Sequencer without utilizing the index scheme.

Index	7	6	5	4	3	2	1	0
6Ch (00)	TMP0							
6Dh (00)	TMP1							
6Eh (00)	TMP2							
6Fh (00)	TMP3							

5.6 I/O Port 60h

Port 60h and 64h are used to emulate the registers of keyboard controller for the generation of a fast gate A20 signal. The sequence is BIOS transparent and there is no need for the modification of the current BIOS. The sequence is to first write data "D1h" to port 64h followed by writing data "02h" to port 60h. Both of these cycles appear on the AT bus.

5.7 I/O Port 61h (Port B)

Bit	Read/Write	Function	Description
7	R	System Parity Check.	1 = Parity Error
6	R	I/O Channel Check.	1 = Channel Check
5	R	Timer OUT2 Detect.	1 = Timer OUT2 is high
4	R	Refresh Detect.	0 = Refresh Request active
3	R/W	I/O Channel Check Enable.	0 = Channel Check enabled
2	R/W	Watchdog Timer Enable.	0 = Watchdog Timer is on
1	R/W	Speaker Output Enable.	1 = Speaker Data enabled
0	R/W	Timer 2 Gate.	1 = Timer 2 Speaker Gate Enabled

5.8 I/O Port 64h

I/O port 64h is used to emulate the register inside the keyboard controller to generate a fast reset pulse. Fast reset pulse is generated by writing data FEh to port 64h. The pulse is generated immediately after the I/O write cycle.

5.9 Port 70h

Bit	Read/Write	Function
7	W	0 = NMI Enable

5.10 Port 92h - System Controller Port A, PS/2 Compatibility Port

Bit	Read/Write	Function
1	R/W	1 = Set Alternate Fast GATEA20 Active
0	R/W	1 = Set Alternate Fast Reset Active

5.11 Registers of '206 portion

5.11.1 Port 96h Shadow Register Definition

Bit	Description	Default
[7:6]	Unused	xx
5	Timer 1 Counter 2 read LSB toggle bit	0
4	Timer 1 Counter 1 read LSB toggle bit	0
3	Timer 1 Counter 0 read LSB toggle bit	0
2	Timer 1 Counter 2 write LSB toggle bit	0
1	Timer 1 Counter 1 write LSB toggle bit	0
0	Timer 1 Counter 0 write LSB toggle bit	0

Note: This feature is supported only when the '206 Register at address 43h, the Read/Write Counter Command Register has been initialized. Register 43h bits [5:4] are set to '11' (03h) to start the sequence. First, read or write the Port 96h LSB bits first, followed by the MSB bits second.

The corresponding bit in Register 96h will be set if the read/write operation is performed, but no MSB operation is performed. If the read/write LSB operation and the the MSB operation are performed correctly, the corresponding bit in Register 96h will be reset to 0.

Please refer to the 82C206 manual for additional detail.

6. 82C463 Pin Cross Reference list and Signal Characteristics Table

Pin	Signal	I/O	mA	Suspend -mode
1	SDIR1	O	4	DL
2	CD16	I/O	4	T
3	MP2/STRAP2	I/O	4	T
4	CD15	I/O	4	T
5	CD14	I/O	4	T
6	CD13	I/O	4	T
7	CD12	I/O	4	T
8	CD11	I/O	4	T
9	CD10	I/O	4	T
10	VCC			
11	CD9	I/O	4	T
12	CD8	I/O	4	T
13	MP1/STRAP1	I/O	4	T
14	CD7	I/O	4	T
15	GND			
16	CD6	I/O	4	T
17	CD5	I/O	4	T
18	CD4	I/O	4	T
19	CD3	I/O	4	T
20	CD2	I/O	4	T
21	CD1	I/O	4	T
22	CD0	I/O	4	T
23	MP0/STRAP0	I/O	4	T
24	RAS3#	O	8	
25	KBDCS#/DWE#	O	8	T
26	GND			
27	CAS3#	O	16	
28	RAS2#	O	8	
29	RAS1#	O	8	
30	RAS0#	O	8	
31	MA9/CSG1#	O	8	
32	MA10	O	8	
33	LOWBAT	I		
34	MA8/CSG0#	O	8	
35	MA7/PPWR7	O	8	
36	MA6/PPWR6	O	8	
37	CAS2#	O	16	
38	GND			
39	CAS1#	O	16	
40	MA5/PPWR5	O	8	
41	MA4/PPWR4	O	8	
42	MA3/PPWR3	O	8	
43	VCC			
44	MA2/PPWR2	O	8	
45	CA31	I		
46	CA24	I		
47	CA23	I/O	4	T
48	CA22	I/O	4	T
49	MA1/PPWR1	O	8	
50	MA0/PPWR0	O	8	
51	CAS0#	O	16	
52	GND			

Pin	Signal	I/O	mA	Suspend -mode
53	VCC			
54	CA21	I/O	4	T
55	CA20	I/O	4	T
56	CA19	I/O	4	T
57	CA18	I/O	4	T
58	CA17	I/O	4	T
59	CA16	I/O	4	T
60	GND			
61	VCC			
62	CA15	I/O	4	T
63	CA14	I/O	4	T
64	CA13	I/O	4	T
65	CA12	I/O	4	T
66	CA11	I/O	4	T
67	CA10	I/O	4	T
68	CA9	I/O	4	T
69	CA8	I/O	4	T
70	CA7	I/O	4	T
71	GND			
72	CA6	I/O	4	T
73	CA5	I/O	4	T
74	CA4	I/O	4	T
75	CA3	I/O	4	T
76	CA2	I/O	4	T
77	DACKMUX2	O	4	T
78	DACKMUX1	O	4	T
79	DACKMUX0/STRAP7	O	4	T
80	DACK2#	O	4	T
81	RQMX3	I		
82	RQMX2	I		
83	RQMX1	I		
84	RQMX0	I		
85	IRQ11	I		
86	IRQ9	I		
87	IRQ5	I		
88	DREQ2	I		
89	CA25/RDYI#	I		
90	LDEV#	I		
91	SD15	I/O	8	T
92	SD14	I/O	8	T
93	SD13	I/O	8	T
94	SD12	I/O	8	T
95	SD11	I/O	8	T
96	GND			
97	VCC			
98	SD10	I/O	8	T
99	SD9	I/O	8	T
100	SD8	I/O	8	T
101	SD7	I/O	8	T
102	SD6	I/O	8	T
103	SD5	I/O	8	T
104	SDEN#	O	4	DL

Note: "T" = Tri-state, "DL" = Drive Low

6. 82C463 Pin Signal Characteristics Table (cont')

Pin	Signal	I/O	mA	Suspend -mode
105	GND			
106	SD4	I/O	8	T
107	SD3	I/O	8	T
108	SD2	I/O	8	T
109	SD1	I/O	8	T
110	SD0	I/O	8	T
111	ADS#	I/O	4	T
112	BLAST#/NPBUSY#	I		
113	BRDY#/ERROR#	I/O	4	
114	VCC			
115	HOLD	O	4	
116	RDY#	I/O	4	T
117	KEN#	O	4	
118	STPCLK	O	4	
119	GND			
120	NMI	O	4	
121	INTR	O	4	
122	SRESET	O	4	
123	AHOLD	O	4	
124	BE0#	I/O	4	T
125	BE1#	I/O	4	T
126	BE2#	I/O	4	T
127	BE3#	I/O	4	T
128	HLDA	I		
129	FERR#	I		
130	A20M#/GA20	I/O	4	DL
131	D/C#	I		
132	W/R#	I/O	4	T
133	M/IO#	I/O	4	T
134	EADS#/NPRST#	O	4	
135	FLUSH#/SMIRDY#	O	4	
136	SMIACT#/SMIADS#	I		
137	SMI#	I/O	4	
138	IGNNE#/BUSY#	O	4	
139	ROMCS#/RTCD#	O	4	T
140	XDIR	O	4	DL
141	CPUCLK	O	8	
142	GND			
143	CLK2OUT	O	8	
144	CLK2IN	I		
145	RFSH#	I/O	8	T
146	SA0/STRAP4	I/O	8	T
147	VCC			
148	SA1/STRAP5	I/O	8	T
149	LCLK	O	8	
150	CHRDY#	I/O	8	T
151	IOWR#	I/O	8	T
152	IORD#	I/O	8	T
153	MWR#	I/O	8	T
154	MRD#	I/O	8	T
155	ATCLK	O	8	
156	GND			

Pin	Signal	I/O	mA	Suspend -mode
157	VCC			
158	KBCLK	O	4	
159	M16#	I/O	8	T
160	LMEGCS#/ATCYC#	O	4	T
161	SBHE#/STRAP6	I/O	8	T
162	BALE	O	8	DL
163	CPURST	O	8	
164	GND	GND		
165	VCC			
166	OSCCLK2	I		
167	KBCLK2	O	4	
168	RTCAS	O	4	DL
169	RST4#	O	4	
170	AEN	O	8	DL
171	PIO3/STPGNT#	I/O	4	
172	PIO2/CPUSPD	I/O	4	
173	PIO1/NOWS#	I/O	4	
174	PIO0	I/O	4	
175	TC	O	4	DL
176	TRIS#	O	4	
177	SPKD	O	4	T
178	IO16#	I		
179	CHCK#	I		
180	OSC14	I		
181	SQWIN	I		
182	LLOWBAT	I		
183	SUSP/RSM	I		
184	EPMI1	I		
185	EPMI2/RSMRST#	I/O	4	
186	MASTER#/RI	I		
187	RST1#	I		
188	PPWRL	O	4	
189	SDIR2	O	4	DL
190	CD31	I/O	4	T
191	CD30	I/O	4	T
192	CD29	I/O	4	T
193	CD28	I/O	4	T
194	CD27	I/O	4	T
195	CD26	I/O	4	T
196	CD25	I/O	4	T
197	CD24	I/O	4	T
198	MP3/STRAP3	I/O	4	T
199	CD23	I/O	4	T
200	GND			
201	VCC			
202	CD22	I/O	4	T
203	CD21	I/O	4	T
204	CD20	I/O	4	T
205	CD19	I/O	4	T
206	CD18	I/O	4	T
207	CD17	I/O	4	T
208	GND			

Note: "T" = Tri-state, "DL" = Drive Low

7. 82C463 Electrical Specification

7.1 DC Characteristics

7.1.1 5V DC Characteristics

(T_A = 0 C to 70 C, V_{CC} = 5V+/- 5%)

Symbol	Description	Min	Max	Units
V_{IH}	Input high voltage	2.0		V
V_{IL}	Input low voltage		0.8	V
V_{OH}	Output high voltage (at rated drive current)	2.4		V
V_{OL}	Output low voltage (at rated drive current)		0.45	V
I_{IH}	Input leakage current, V_{IN} = V_{CC}	-10	10	
I_{IL}	Input leakage current, V_{IN} = GND	-10	10	uA
I_{OZ}	Tri-state leakage current 0.45V < V_{OUT} < V_{CC}	-10	10	uA
I_{CC}	Operating current (suspend mode)		50	uA

7.1.2 3.3V DC Characteristics

(T_A = 0 C to 70 C, V_{CC}= 3.3V+/- 5%)

Symbol	Description	Min	Max	Units
V_{IH}	Input high voltage	2.4		V
V_{IL}	Input low voltage		0.7	V
V_{OH}	Output high voltage (at rated drive current)	2.4		V
V_{OL}	Output low voltage (at rated drive current)		0.40	V
I_{IH}	Input leakage current, V_{IN} = V_{CC}	-10	10	uA
I_{IL}	Input leakage current, V_{IN} = GND	-10	10	uA
I_{OZ}	Tri-state leakage current GND < V_{OUT} < V_{CC}	-10	10	uA
I_{CC}	Operating current (suspend mode)		35	uA

7.2 AC Characteristics

Symbol	Description	Min	Max	Units
C_{IN}	Input capacitance		10	pF
C_{OUT}	Output capacitance		10	pF
C_{IO}	I/O Capacitance		12	pF

7.3 Absolute Maximum Ratings: 5V and 3.3V

Symbol	Description	Min	Max	Units
V_{CC}	Operating voltage	3.0	6.5	V
V_{IH}	Input high voltage	2.4	V_{CC} + 0.3	V
V_{IL}	Input low voltage	-0.3	0.8	V
T_A	Ambient Temperature	0	70	degrees C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded.

8. 82C463 Timing Characteristics

8.1 82C463 5V 33MHz Timing Characteristics

(TA = 0 C to 70 C, Vcc = 5V+/- 5%)

Sym	Description	Min	typ	Max	Units
t101	CLK2IN rising edge to ECLK rising edge	3		8	ns
t102	CLK2IN rising edge to ECLK falling edge	3		8	ns
t103	LDEV# to CLK2IN rising edge setup time	5			ns
t104	LDEV# to CLK2IN rising edge hold time	3			ns
t105	ADS# to CLK2IN rising edge setup time	5			ns
t106	ADS# to CLK2IN rising edge hold time	3			ns
t107	ADDR to CLK2IN rising edge setup time	5			ns
t108	ADDR to CLK2IN rising edge hold time	3			ns
t111	RDY# to CLK2IN setup time	9			ns
t112	RDY# to CLK2IN hold time	6			ns
t113	CLK2IN rising edge to SRESET/CPURST/NPRST active delay	8	10	15	ns
t114	CLK2IN rising edge to SRESET/CPURST/NPRST inactive delay *	8	10	15	ns
t117	NPBUSY# active width	13			ns
t118	FERR# to NPBUSY# hold time	5			ns
t119	FERR# to NPBUSY# setup time	5			ns
t120	NPBUSY# active to BUSY# active delay	8	12		ns
t121	NPBUSY# inactive to BUSY# inactive delay	8	12		ns
t122	FERR# low pulse width	8			ns
t123	IOWR# active to BUSY# inactive delay		12		ns
t125	NPRST active width (to 0F1h)	40 x CLK2IN cycles			
t126	RDYI# to CLK2IN setup time	15			ns
t127	RDYI# to CLK2IN hold time	10			ns

*Note: This timing may not meet CPU specification at 33MHz. Please refer to Product Alert dated 7-6-93 for more details.

8.1 82C463 33MHz 5V Timing Characteristics (continued)
(TA = 0 C to 70 C, Vcc= 5V+/- 5%)

Sym	Description	Min	typ	Max	Units
t201	CAS# inactive pulse width	10			ns
t202	CLK2IN rising edge to CAS# active delay	10	14	19	ns
t203	CLK2IN rising edge to CAS# inactive delay	10	14	18	ns
t204	CLK2IN to RDY# (or BRDY#) active delay	10	17	22	ns
t205	CLK2IN to RDY# (or BRDY#) inactive delay	10	13	19	ns
t206	CLK2IN to RAS# inactive delay	10	12	16	ns
t207	CLK2IN to RAS# active delay	12	16	20	ns
t208	non CPU cycle CMD to RAS# active delay		2		CLK2IN
t209	non CPU cycle CMD inactive to RAS# inactive delay		2		CLK2IN
t210	non CPU cycle RAS active to CAS# address valid		2		CLK2IN
t211	non CPU cycle RAS active to CAS# active delay		4		CLK2IN
t212	non CPU cycle CMD inactive to CAS# inactive delay		2		CLK2IN
t213	non CPU cycle CMD active to DWE# active delay		2		CLK2IN
t214	non CPU cycle CMD inactive to DWE# inactive delay		2		CLK2IN
t215	RFSH# active to CAS0-3# active delay		4		CLK2IN
t216	CAS0-3# active to RAS2#, RAS0# active delay		2		CLK2IN
t217	CAS4-7# active to RAS1#, RAS3# active delay		3		CLK2IN
t218	RAS1,3# active to RAS1#, RAS3# active delay		1		CLK2IN
t219	CLK2IN to DWE# active delay		22	30	ns
t220	CLK2IN to DWE# inactive delay		10	18	ns
t221	CLK2IN to MA[10:0] valid delay	12	24	30	ns
t222	CLK2IN to MA[10:0] change delay	8	17	25	ns
t223	RFSH# active period		4		AT cycle
t224	On-board DRAM refresh period		9		CLK2IN
t225	MA[10:0] to RAS# (CAS#) hold time	15	20		ns
t226	MA[10:0] to CAS# (CAS#) setup time	0	15		ns
t227	RAS# pre-charge time	60			ns
t228	CLK2IN falling edge to CAS# active delay	10	12	19	ns
t229	CLK2IN falling edge to CAS# inactive delay (for read 3-1-1-1 cycle - 25MHz)	14	16	18	ns
t230	CLK2IN rising edge to CAS# active delay (for read 3-1-1-1 cycle - 25MHz)	13	16	20	ns

8.1 82C463 33MHz 5V Timing Characteristics (continued)
(TA = 0 C to 70 C, Vcc= 5V+/- 5%)

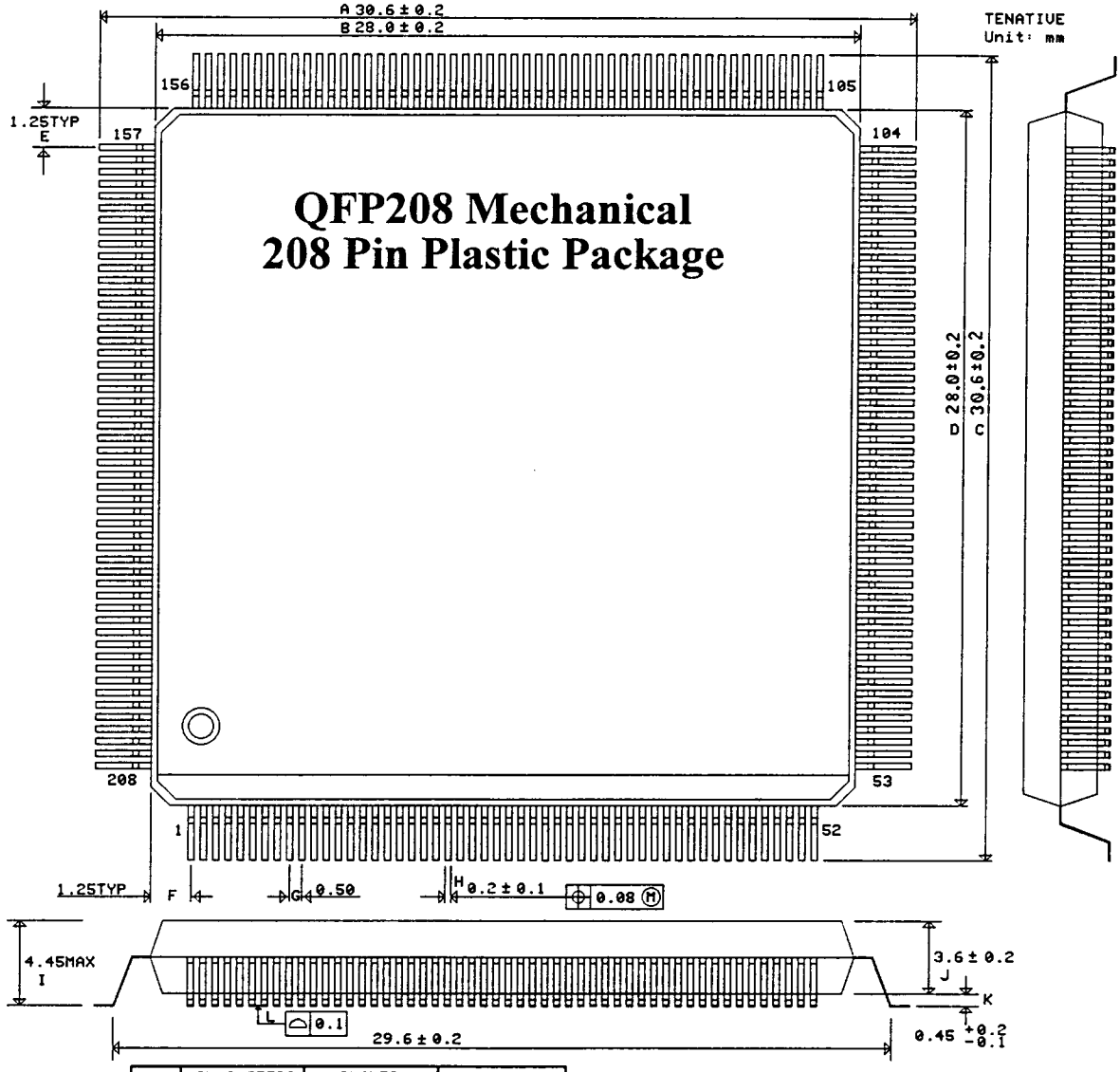
Sym	Description	Min	typ	Max	Units
t301	D(31:0) active to SD(15:0) delay	9		17	ns
t302	D(31:0) active to MP(3:0) delay	8		18	ns
t303	D(31:0) inactive to SD(15:0) delay	8		18	ns
t304	D(31:0) inactive to MP(3:0) delay	8		18	ns
t305	SD(15:0) active to D(31:0) delay	8		16	ns
t306	SD(15:0) active to PM(3:0) delay	12		20	ns
t307	SD(15:0) inactive to D(31:0) delay	8		16	ns
t308	SD(15:0) inactive to MP(3:0) delay	12		20	ns
t309	SD(15:0) to IORD#, MRD# setup time	5			ns
t310	SD(15:0) to IORD#, MRD# hold time	5			ns
t311	SD(15:8) active to SD(7:0) delay	8		16	ns
t312	SD(15:8) inactive to SD(7:0) delay	9		18	ns
t313	CHCK# active to NMI delay		18		ns
t314	IOWR# to NMI, SPKD change		20		ns
t315	SA(1:0) to KBDCS# active delay	10	14		ns
t316	SA(1:0) to KBDCS# inactive delay	10	14		ns

t501	ATCLK falling to ALE active delay		1	2	ns
t502	ATCLK to ALE inactive delay		.8	1.2	ns
t503	ATCLK falling to CMD active delay		2	4	ns
t503.1	ATCLK falling to 16 bit CMD active delay		2	4	ns
t504	ATCLK to CMD inactive delay		2	4	ns
t505	M16# to ATCLK setup time	8			ns
t506	M16# to ATCLK hold time	4			ns
t507	IO16# to ATCLK setup time	10			ns
t508	IO16# to ATCLK hold time	10			ns
t509	NOWS# to ATCLK setup time	9			ns
t510	NOWS# to ATCLK hold time	4			ns
t511	CHRDY to ATCLK setup time	11			ns
t512	CHRDY to ATCLK hold time	4			ns
t513	CLK2IN to HOLD active delay	6	10		ns
t514	CLK2IN to HOLD inactive delay	5	9		ns
t516	ATCLK to RFSH# inactive delay	20	30		ns
t517	ATCLK to MRD# active delay	3	5		ns
t518	ATCLK to MRD# inactive delay	8	15		ns
t523	CLK2IN to SDIR1, SDIR2 active delay		12	15	ns
t524	CLK2IN to SDIR1, SDIR2 inactive delay		13	15	ns
t525	CLK2IN to SDEN active delay		15	25	ns
t526	CLK2IN to SDEN inactive delay		16	25	ns
t527	NPBUSY# to FERR# setup time	3			ns

8.2 82C463 3.3V 25MHz Timing Characteristics

This section will be published at a later date.

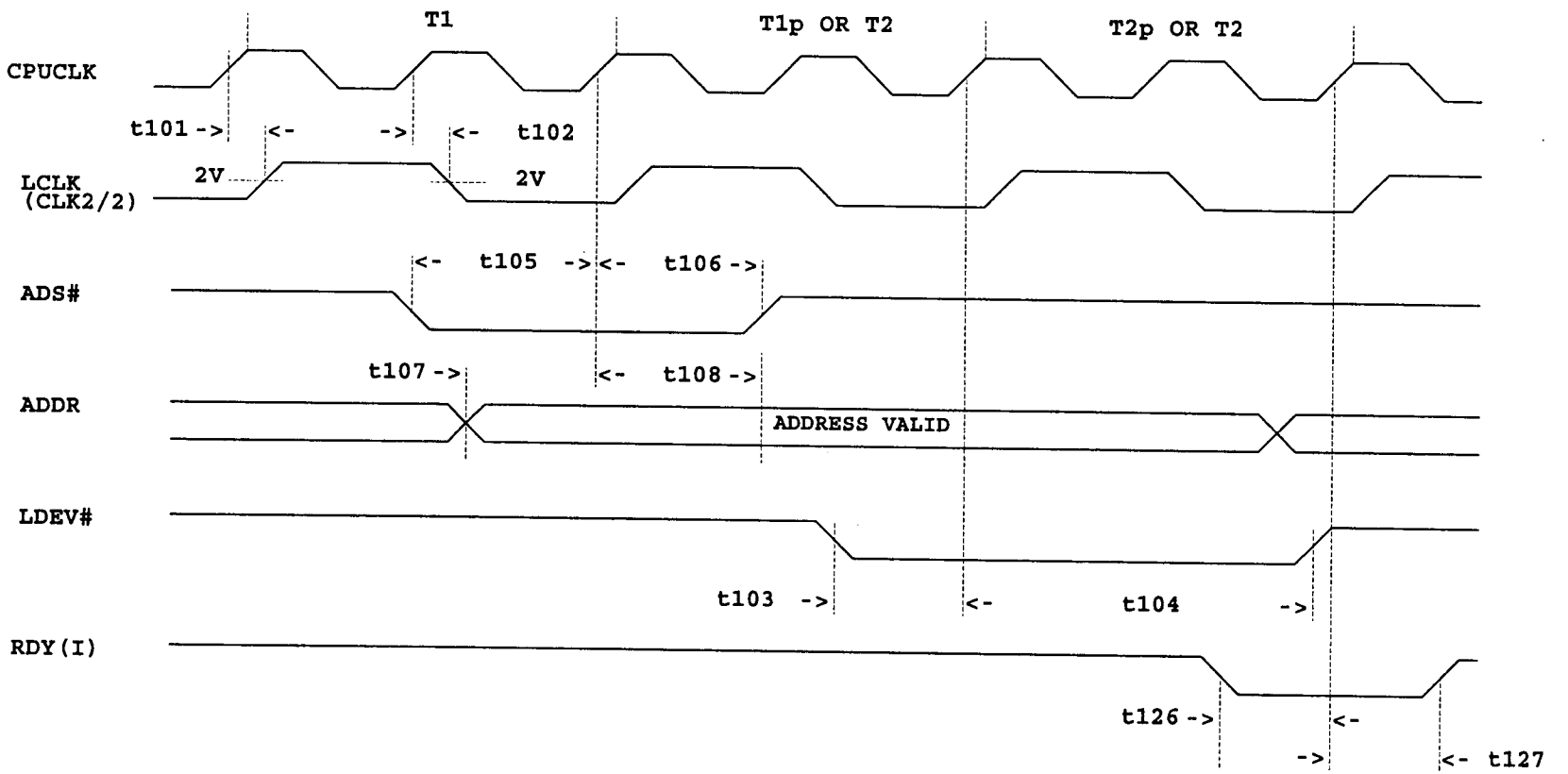
9. 82C463 Mechanical Package



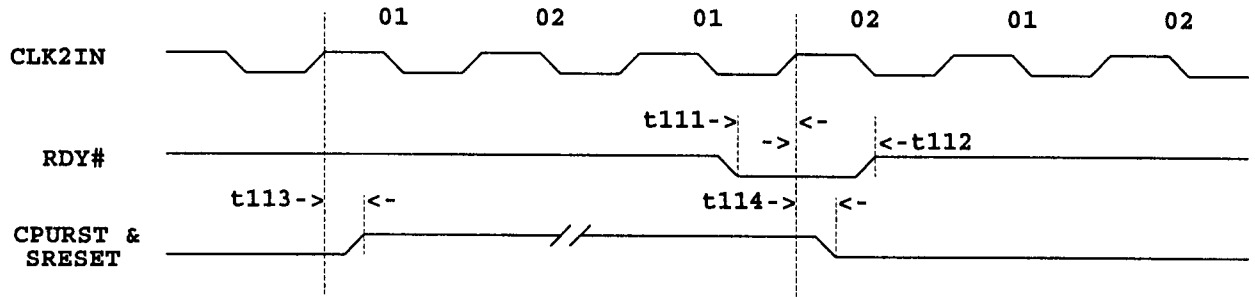
DIM	MILLIMETERS		INCHES		DESCRIPTION
	MIN	MAX	MIN	MAX	
A	30.4	30.8	1.197"	1.213"	Maximum Width LEAD TO LEAD
B	27.8	28.2	1.094"	1.110"	Maximum Width PACKAGE ENVELOPE
C	30.4	30.8	1.197"	1.213"	Maximum Height LEAD TO LEAD
D	27.8	28.2	1.094"	1.110"	Maximum Height PACKAGE ENVELOPE
E	1.25 TYP		.0495" TYP		LEAD CENTER TO PERP. LEAD PLANE
F	1.25 TYP		.0495" TYP		LEAD CENTER TO PERP. LEAD PLANE
G	0.5		.0197"		LEAD TO LEAD CENTER SPACING
H	0.1	0.3	.004"	.012"	LEAD WIDTH
I	——	4.45	——	.175"	PACKAGE HEIGHT LEAD PLANE TO TOP
J	3.4	3.8	.134"	.150"	MAXIMUM THICKNESS PACKAGE ENVELOPE
K	0.35	0.65	.0138"	.0256"	LEAD PLANE TO PACKAGE BOTTOM
L	——	0.1	——	.004"	LEAD PLANE SKEW
M	0.1	0.25	.004"	.01"	LEAD THICKNESS
N	0.3	0.7	.012"	.028"	LEAD FOOTPRINT

10. Timing Diagrams

10.1 CPU Single Cycle Timing

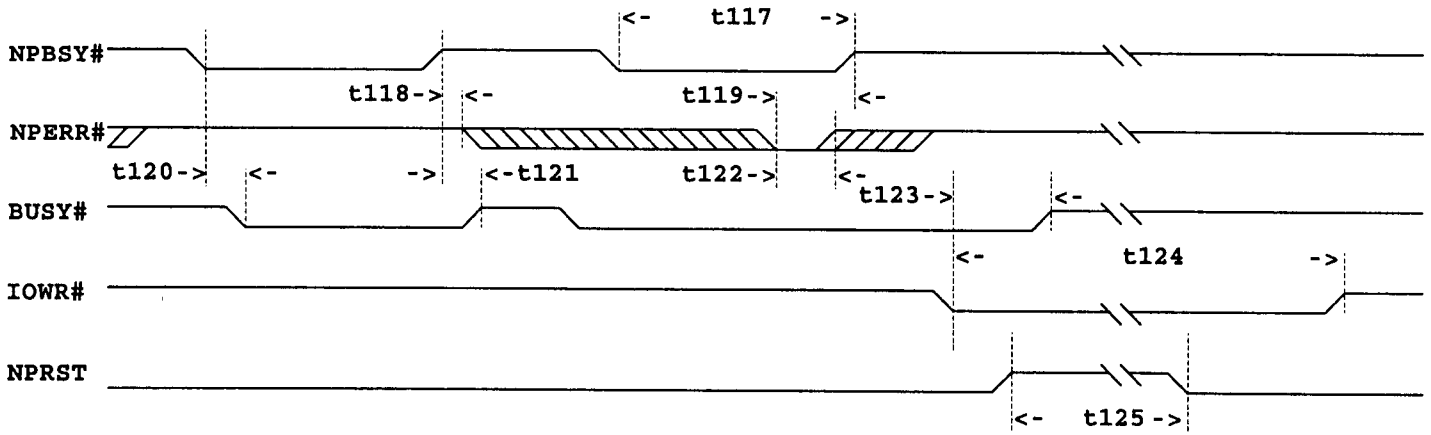


10.2 Reset Timing



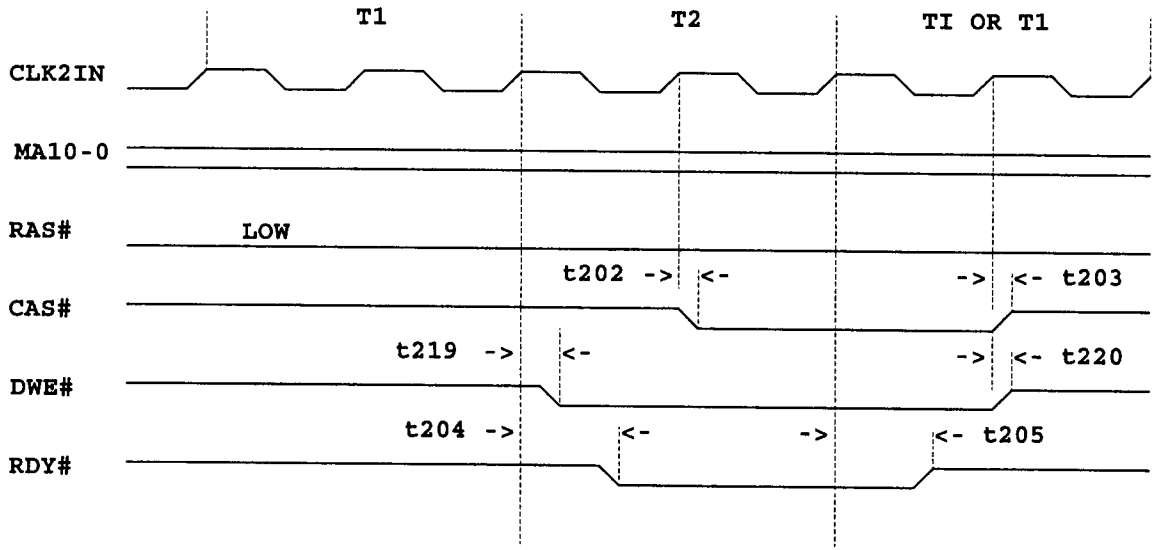
RESET TIMING

10.3 Numerical Processor Reset Timing



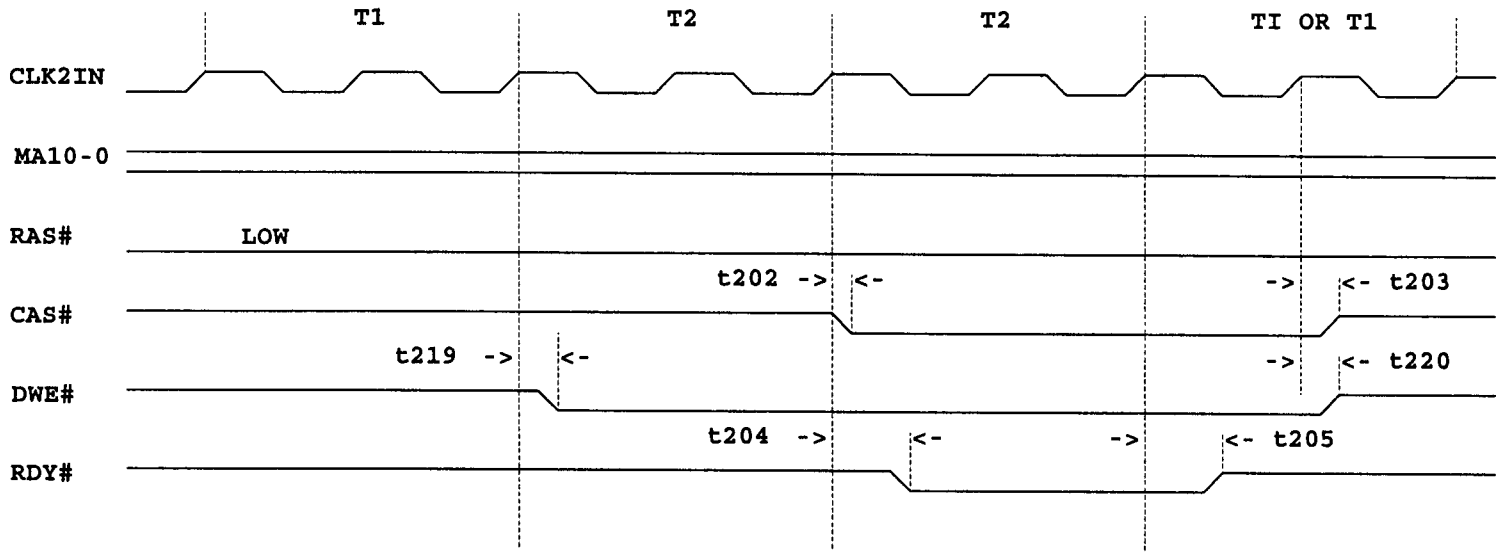
387 NUMERICAL PROCESSOR RESET TIMING

10.4 Write Cycle, Page Hit, 0 Wait State



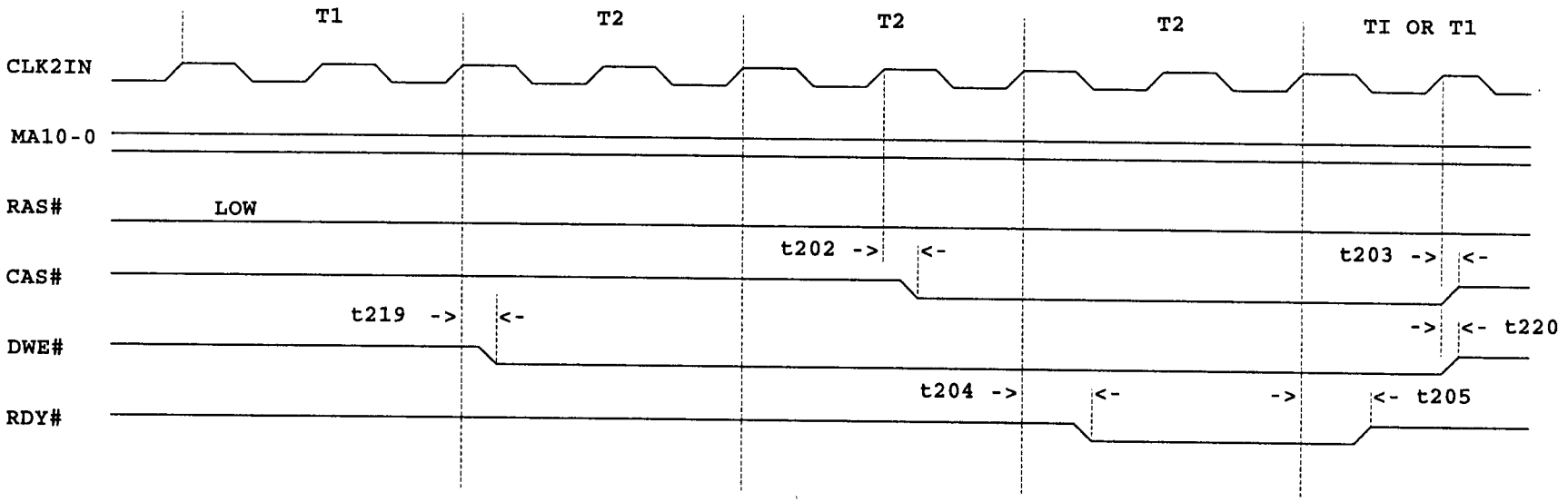
WRITE CYCLE, PAGE HIT, 0 WAIT STATE

10.5 Write Cycle, Page Hit, 1 Wait State (or Read = 4-3-3-3, Write = 1 WS)



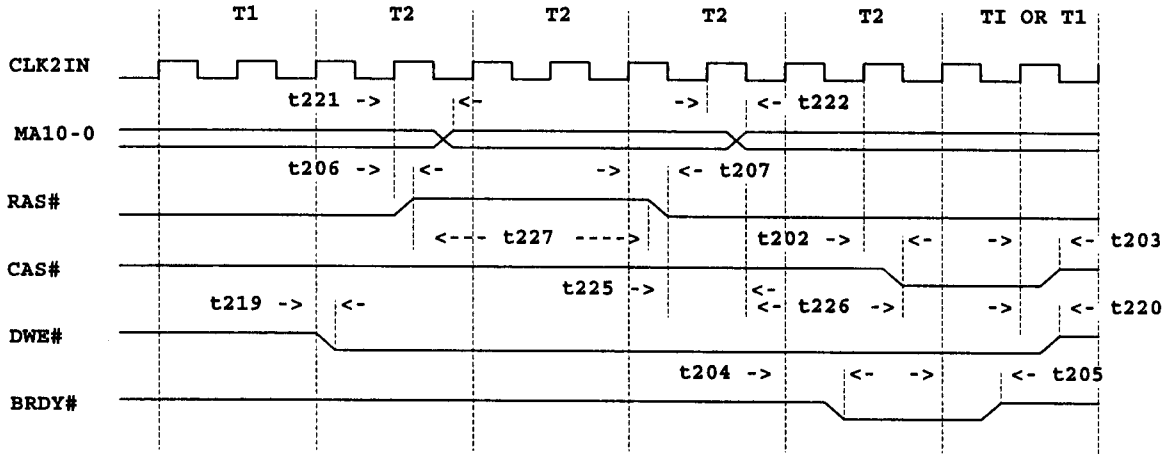
WRITE CYCLE, PAGE HIT, 1 WAIT STATE
(OR READ = 4-3-3-3, WRITE = 1WS)

10.6 Write Cycle, Page Hit, 2 Wait States



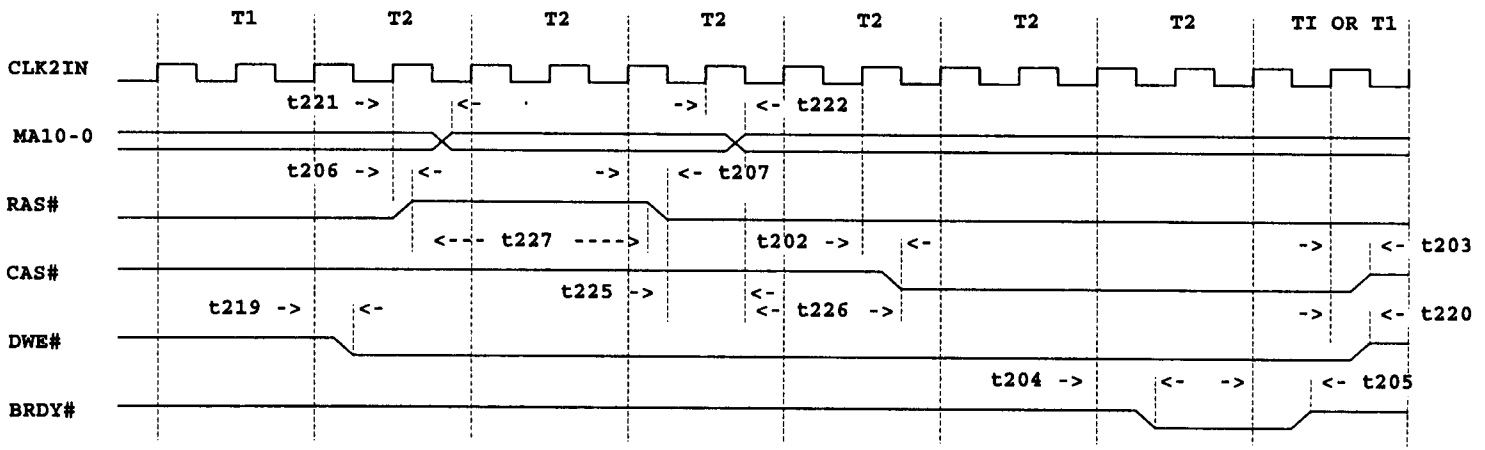
WRITE CYCLE, PAGE HIT, 2 WAIT STATES

10.7 Write Cycle, 0/1 Wait State, Page Miss, Read = 2-1-1-1 (20MHz) or 3-1-1-1 (25MHz)



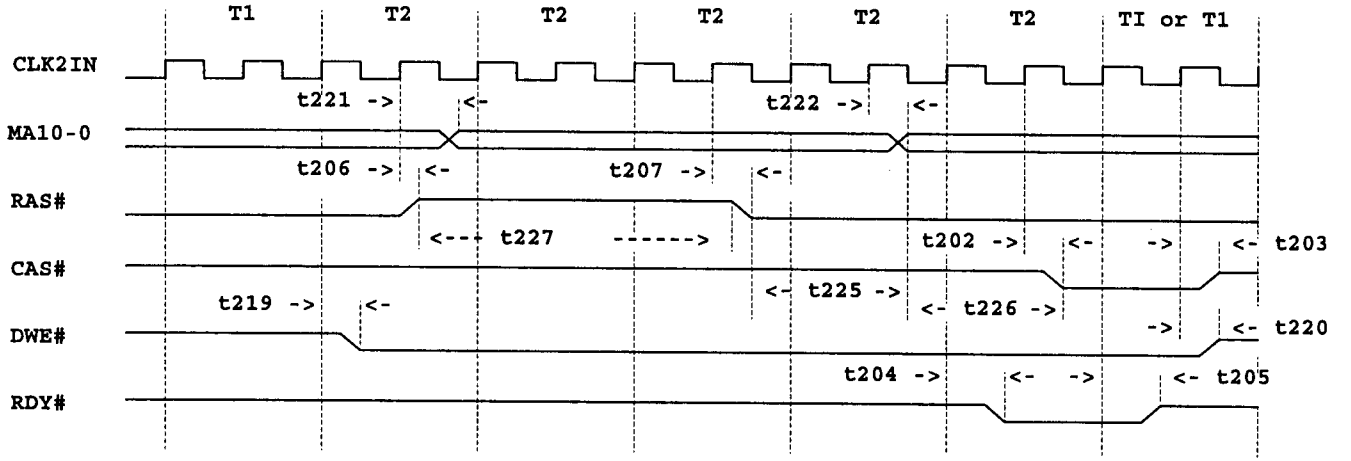
WRITE = 0 OR 1 WS, PAGE MISS
(WITH READ = 2-1-1-1 OR 3-1-1-1)

10.8 Write Cycle, 2 Wait States, Page Miss, Read = 2-1-1-1 (20MHz) or 3-1-1-1 (25MHz)



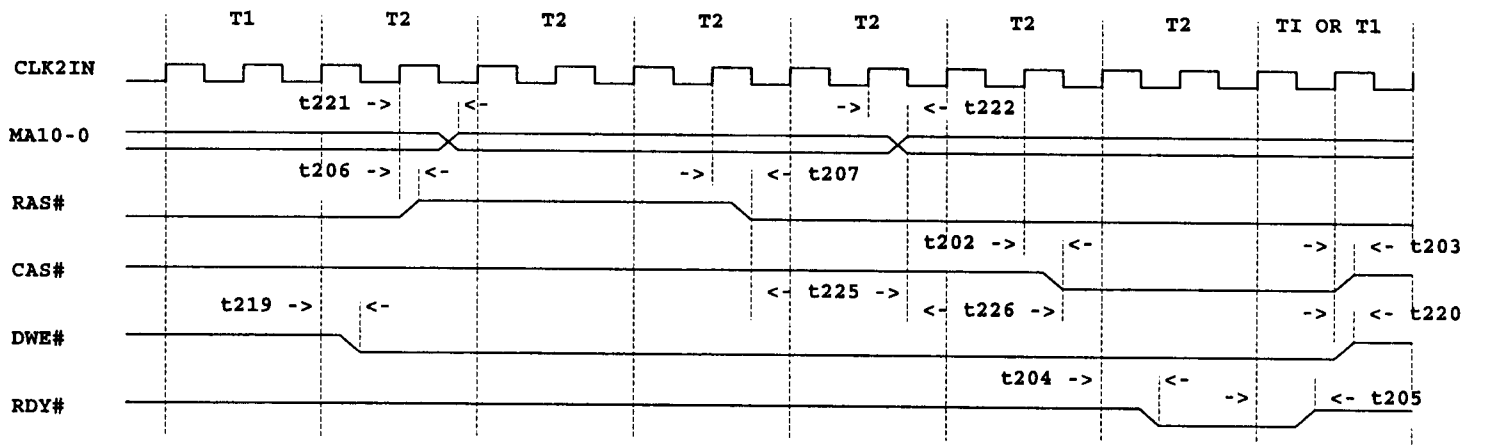
WRITE = 2 WS, PAGE MISS
(WITH READ = 2-1-1-1 OR 3-1-1-1)

10.9 Write Cycle, 0 or 1 Wait State, Page Miss, Read = 3-2-2-2 (33 MHz)



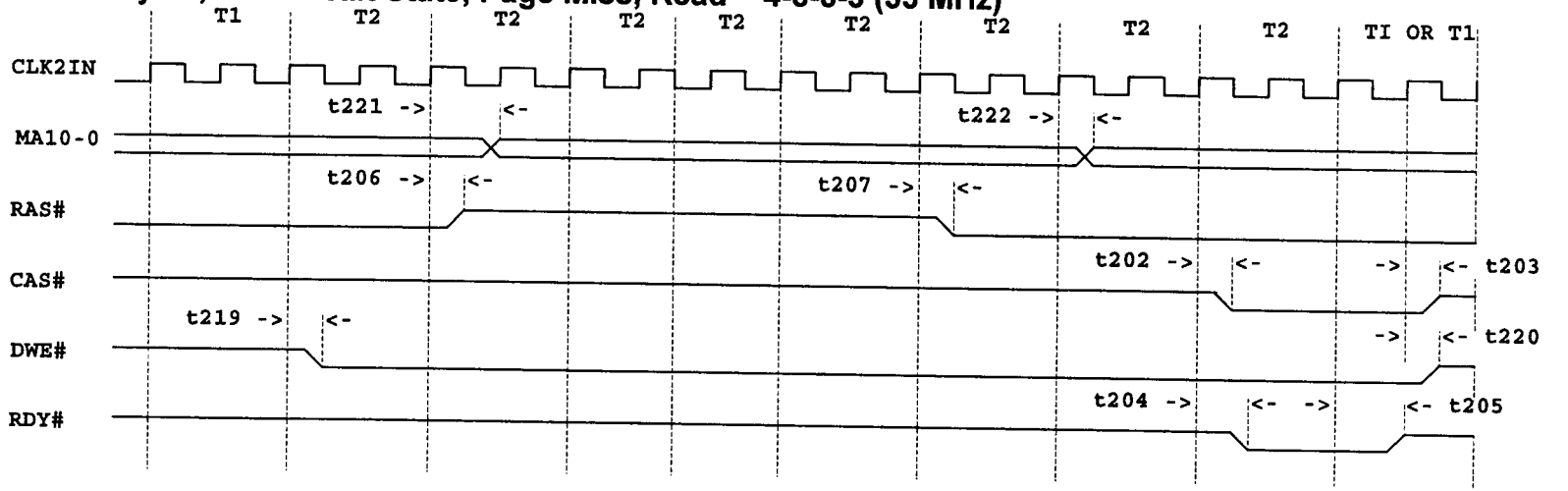
WRITE = 0 OR 1 WS, PAGE MISS
(WITH READ = 3-2-2-2)

10.10 Write Cycle, 2 Wait States, Page Miss, Read = 3-2-2-2 (33 MHz)



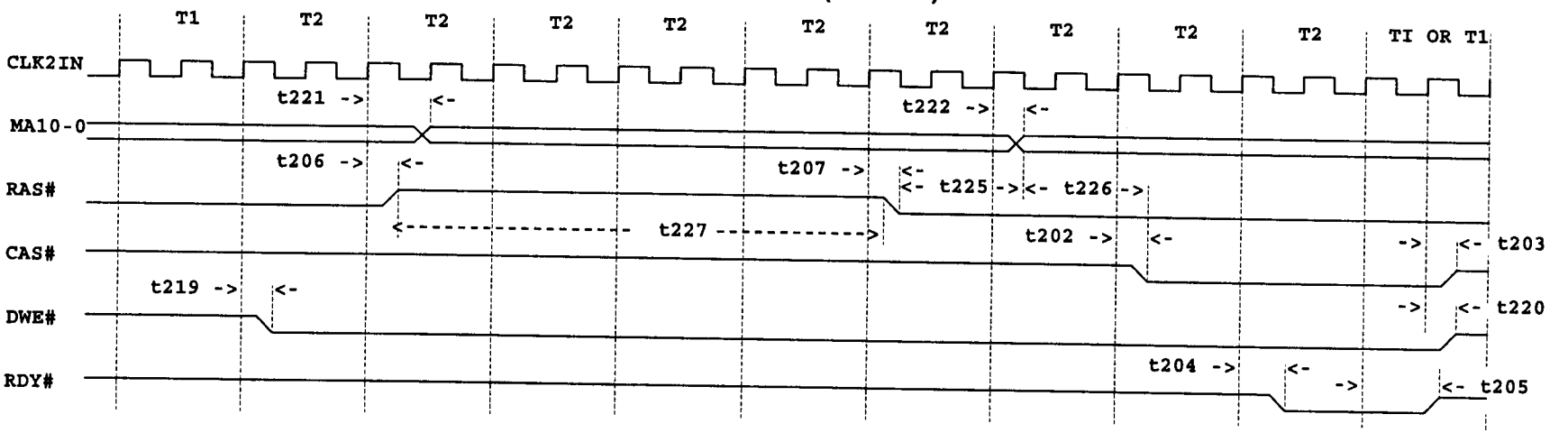
WRITE = 2 WS, PAGE MISS
(WITH READ = 3-2-2-2)

10.11 Write Cycle, 0 or 1 Wait State, Page Miss, Read = 4-3-3-3 (33 MHz)



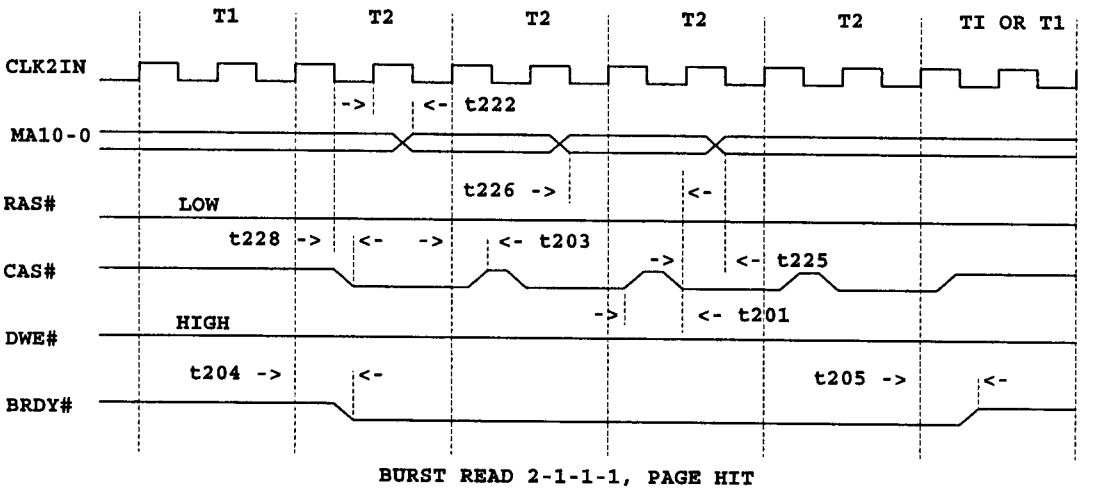
WRITE = 0 OR 1 WS, PAGE MISS (WITH READ = 4-3-3-3)

10.12 Write Cycle, 2 Wait States, Page Miss, Read = 4-3-3-3 (33 MHz)



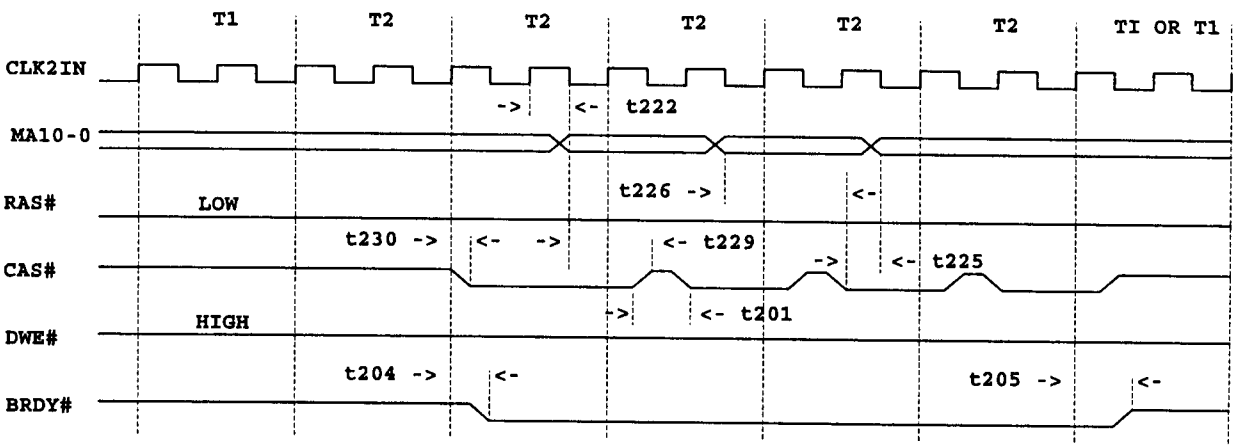
WRITE = 2 WS, PAGE MISS (WITH READ = 4-3-3-3)

10.13 Burst Read Cycle, 2-1-1-1 (20 MHz), Page Hit



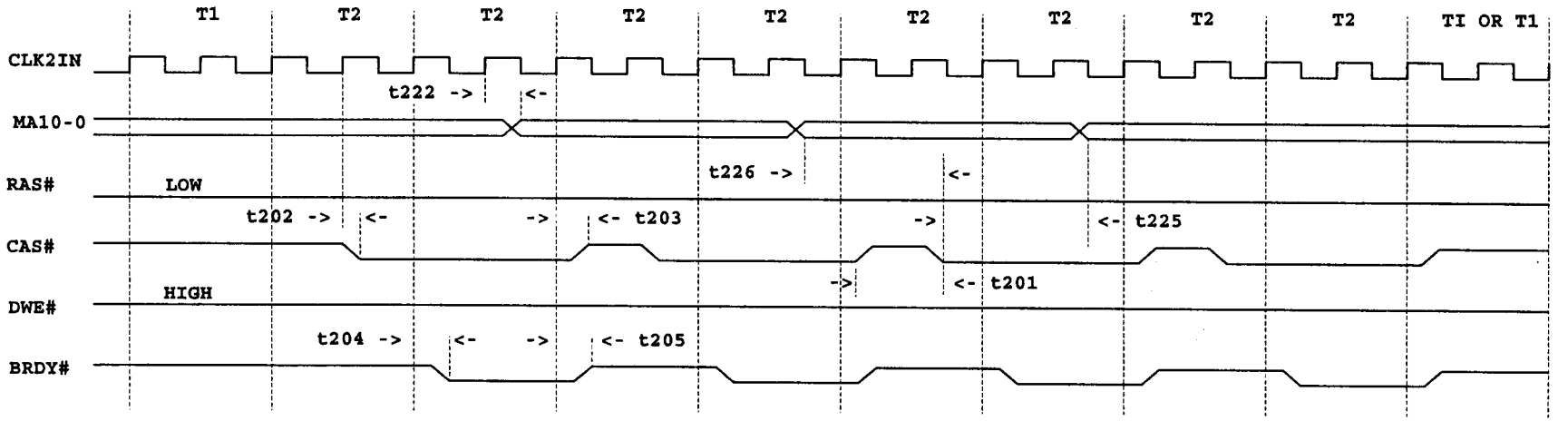
BURST READ 2-1-1-1, PAGE HIT

10.14 Burst Read Cycle, 3-1-1-1 (25 MHz), Page Hit



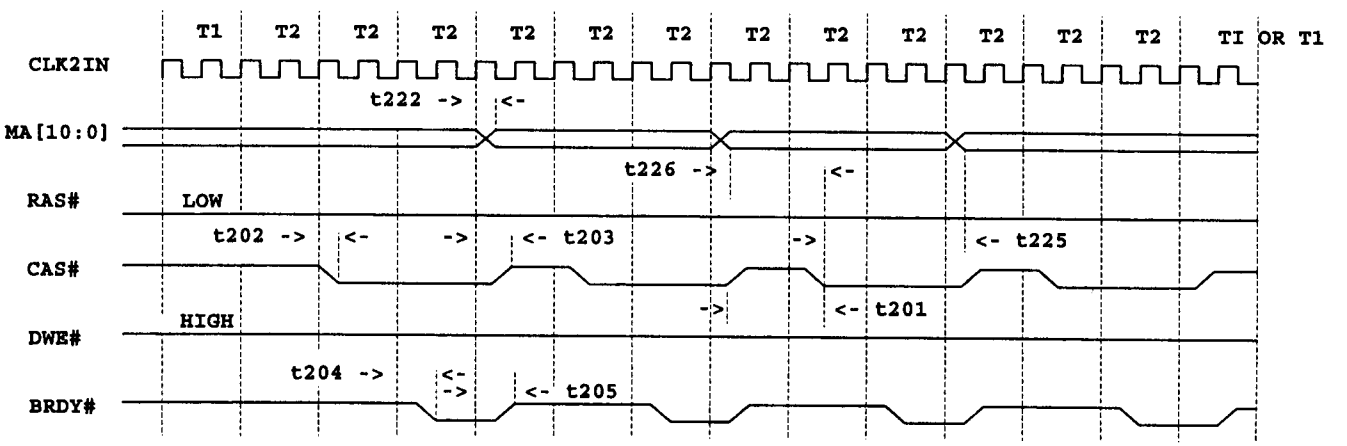
BURST READ 3-1-1-1, PAGE HIT

10.15 Burst Read Cycle, 3-2-2-2 (33 MHz), Page Hit



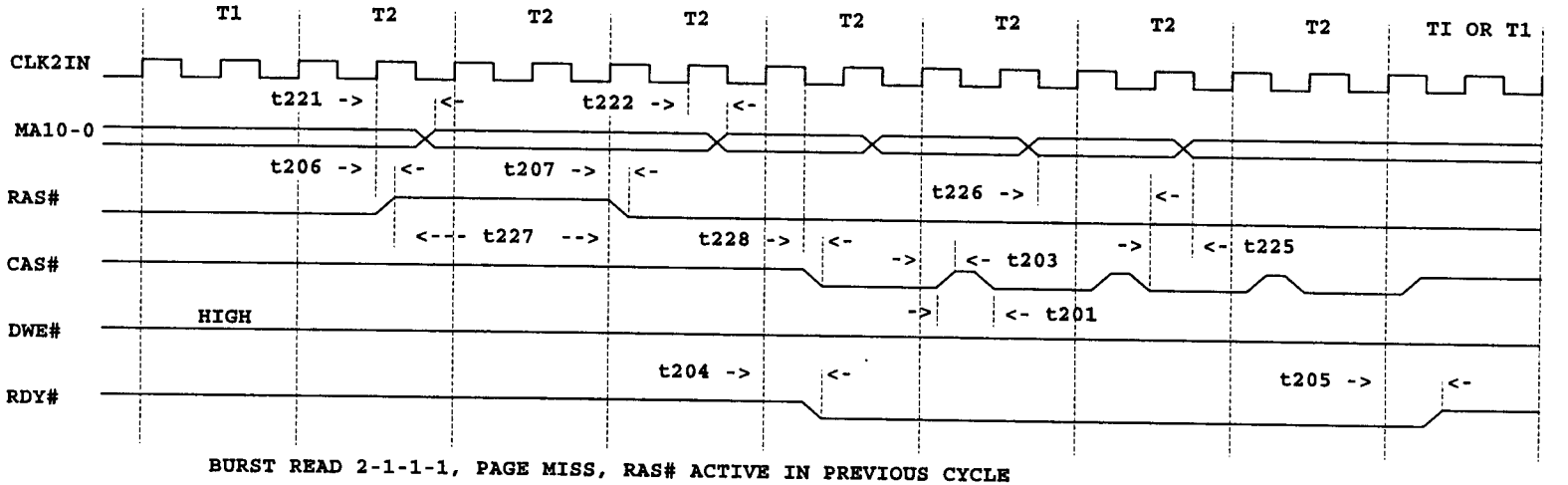
BURST READ 3-2-2-2, PAGE HIT

10.16 Burst Read Cycle, 4-3-3-3 (33 MHz), Page Hit



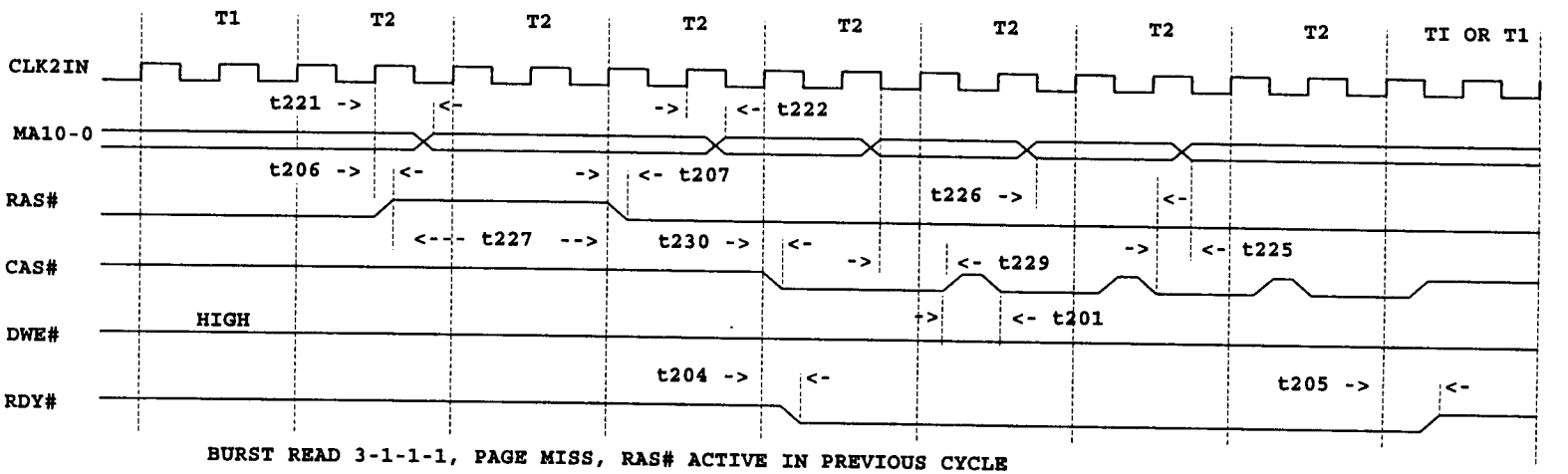
BURST READ 4-3-3-3, PAGE HIT

10.17 Burst Read Cycle, 2-1-1-1 (20 MHz), Page Miss, RAS# Active in Previous Cycle



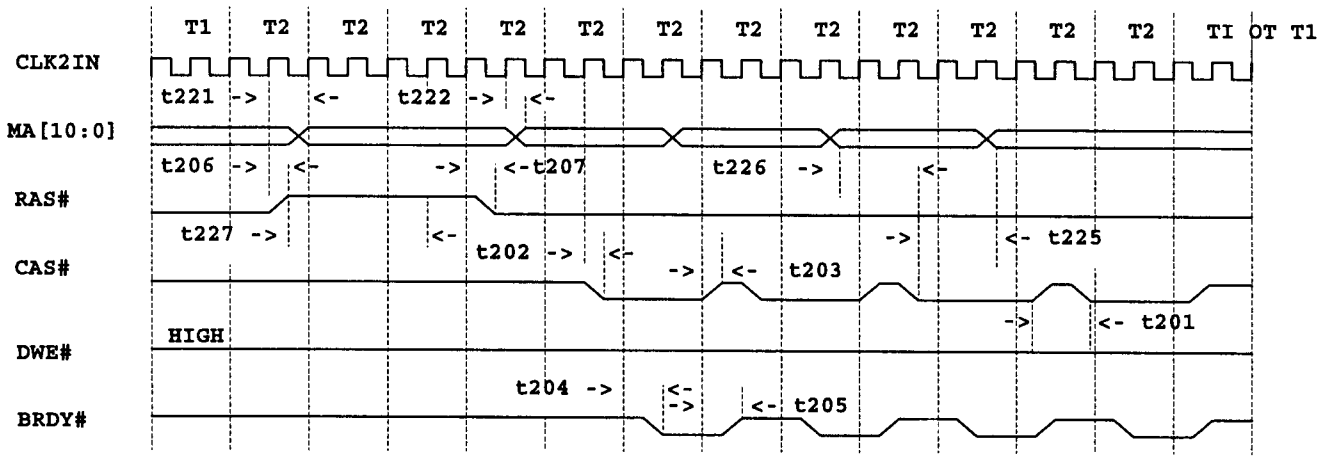
BURST READ 2-1-1-1, PAGE MISS, RAS# ACTIVE IN PREVIOUS CYCLE

10.18 Burst Read Cycle, 3-1-1-1 (25 MHz), Page Miss, RAS# Active in Previous Cycle



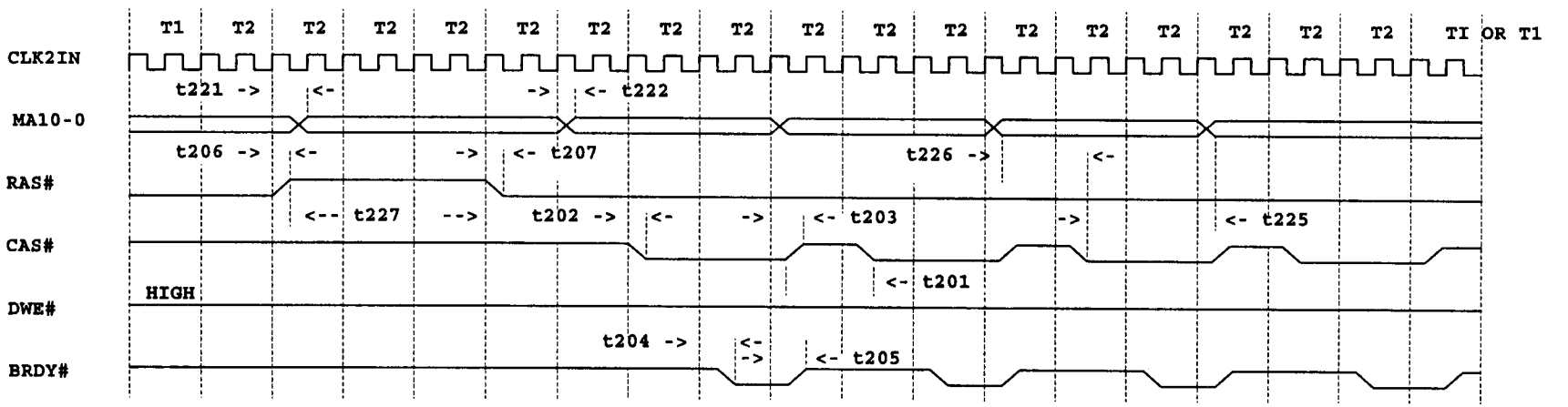
BURST READ 3-1-1-1, PAGE MISS, RAS# ACTIVE IN PREVIOUS CYCLE

10.19 Burst Read Cycle, 3-2-2-2 (33 MHz), Page Miss, RAS# Active in Previous Cycle



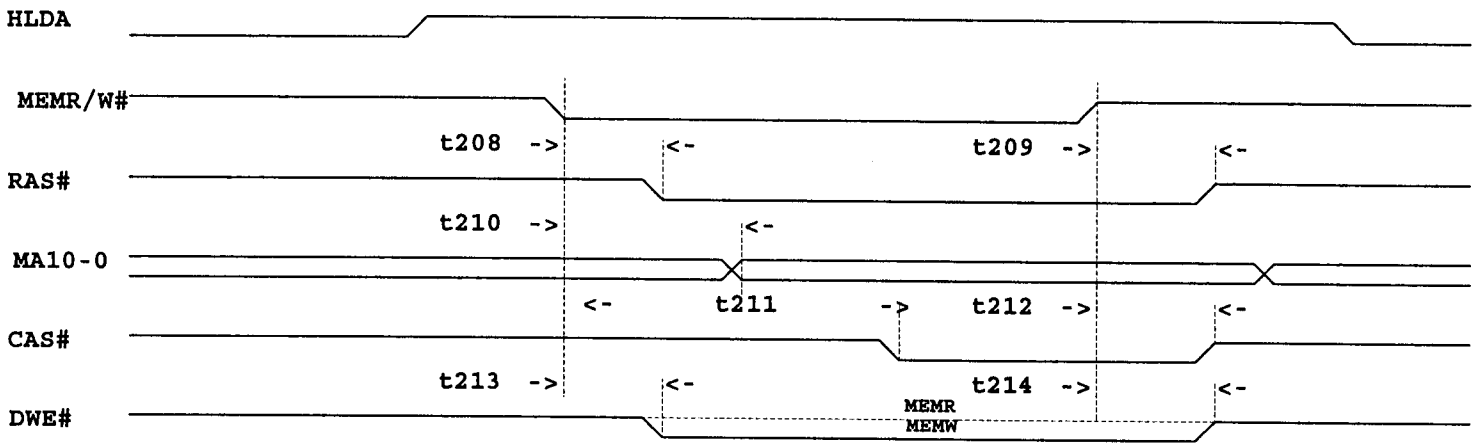
BURST READ 3-2-2-2, PAGE MISS, RAS# ACTIVE IN PREVIOUS CYCLE

10.20 Burst Read Cycle, 4-3-3-3 (33 MHz), Page Miss, RAS# Active in Previous Cycle



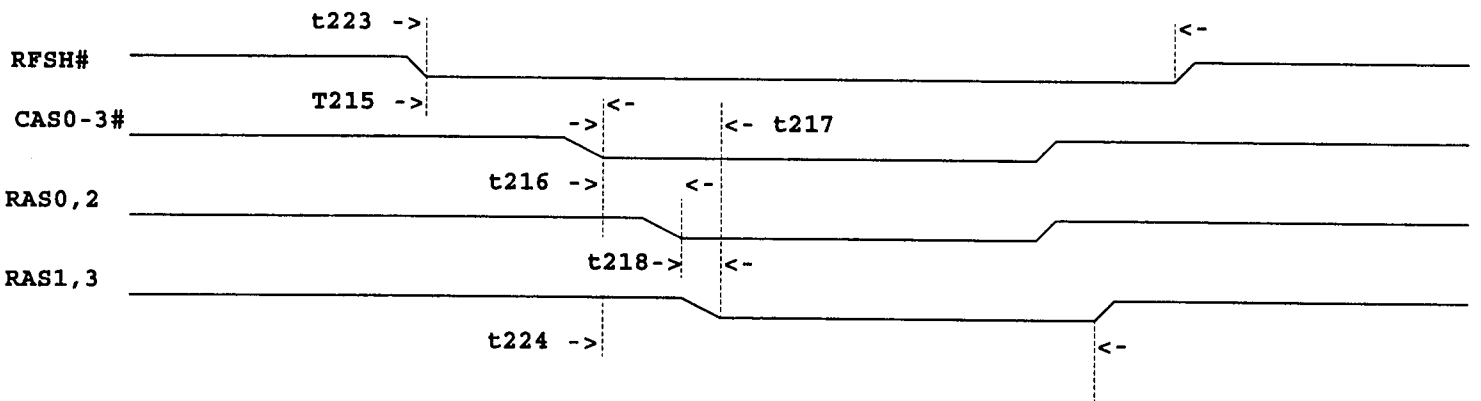
BURST READ 4-3-3-3, PAGE MISS, RAS# ACTIVE IN PREVIOUS CYCLE

10.21 DMA / MASTER Cycle



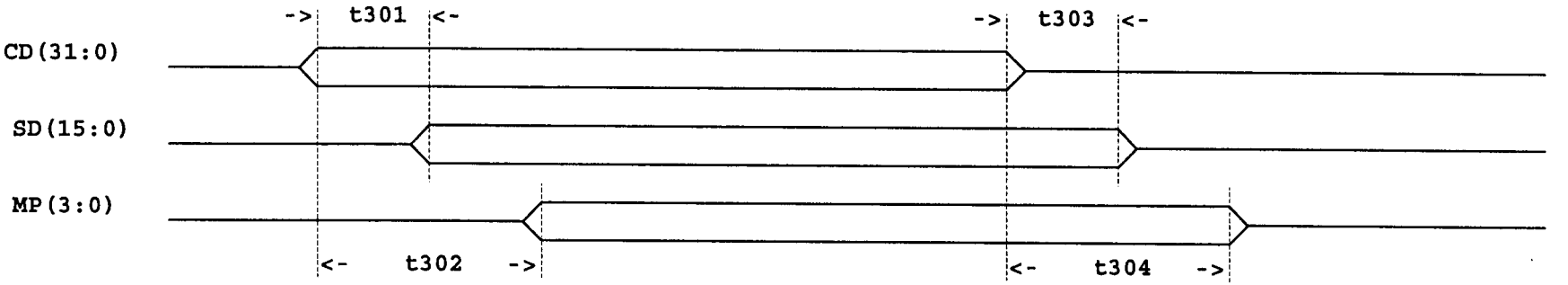
DMA/MASTER CYCLE

10.22 Normal Refresh Cycle



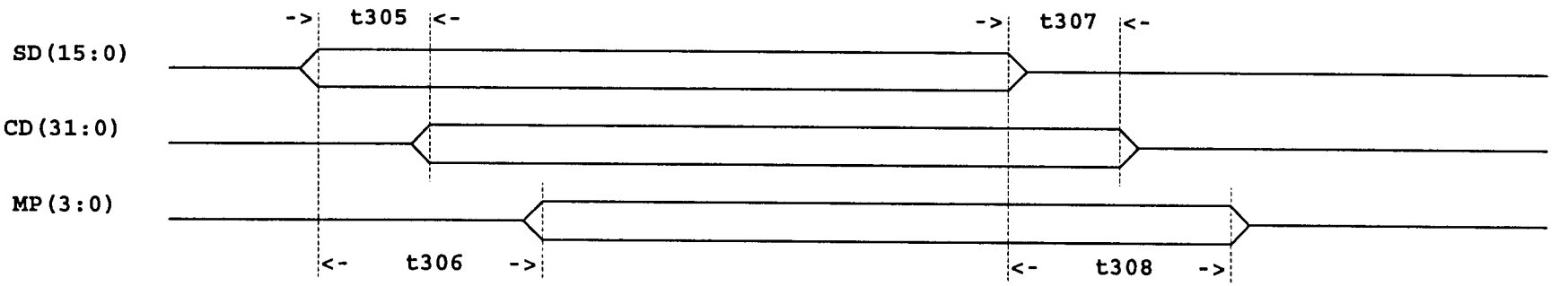
Normal Refresh Cycle

10.23 CD[31:0] to SD[15:0] & MP[3:0] Valid and Invalid Delay



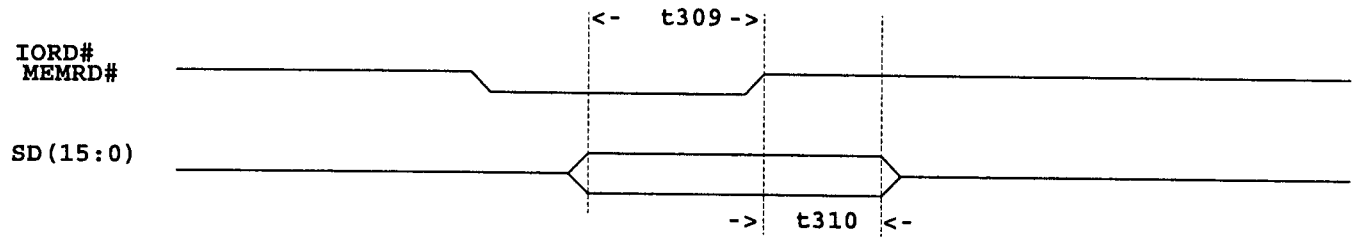
CD(31:0) TO SD(15:0) & MP(3:0) VALID AND INVALID DELAY

10.24 SD[15:0] to CD[31:0] & MP[3:0] Valid and Invalid Delay



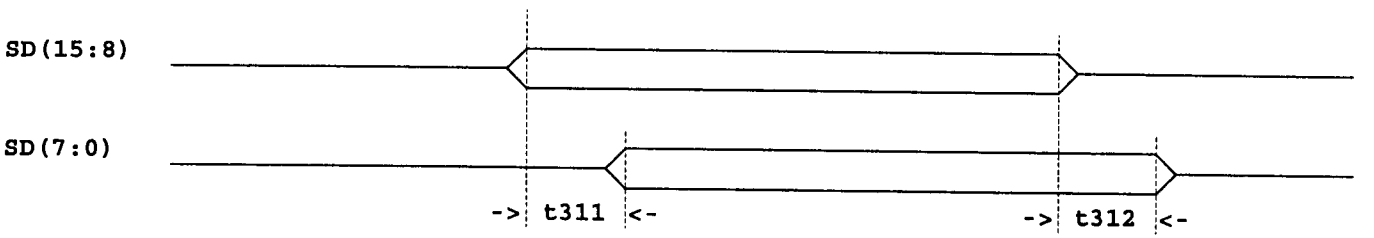
SD(15:0) TO CD(31:0) & MP(3:0) VALID AND INVALID DELAY

10.25 Data Setup and Hold Time for IORD# and MEMRD#



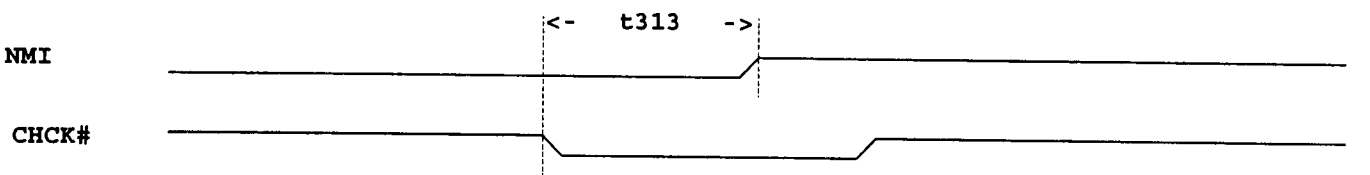
DATA SETUP AND HOLD TIME FOR IORD# AND MEMRD#

10.26 Data Valid and Invalid Delay Between SD[15:8] and SD[7:0]



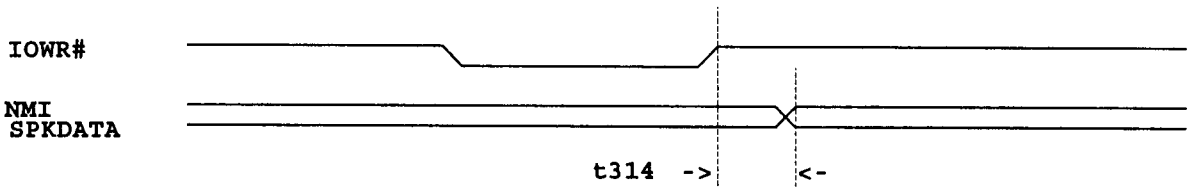
DATA VALID AND INVALID DELAY BETWEEN SD(15:8) AND SD(7:0) SWAPPING

10.27 NMI Valid Delay Related to CHCK#



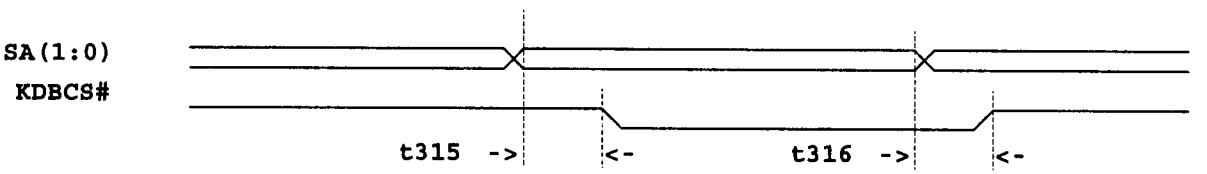
NMI VALID DELAY RELATED TO CHCK#

10.28 Value Change Delays for IOP61 and IOP70 Controlled Outputs



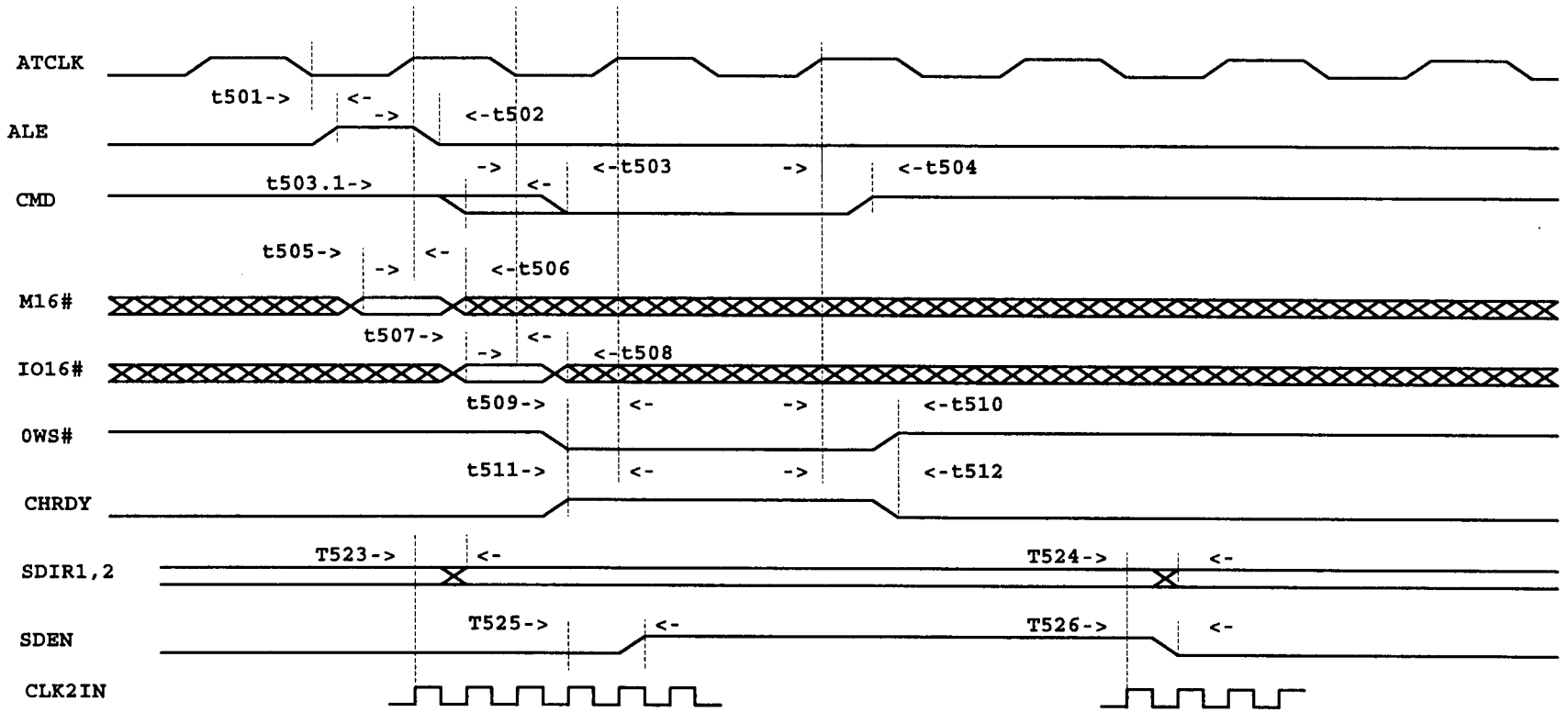
VALUE CHANGE DELAYS FOR IOP61 AND IOP70 CONTROLLED OUTPUTS

10.29 KBDCS# Valid and Invalid Delay



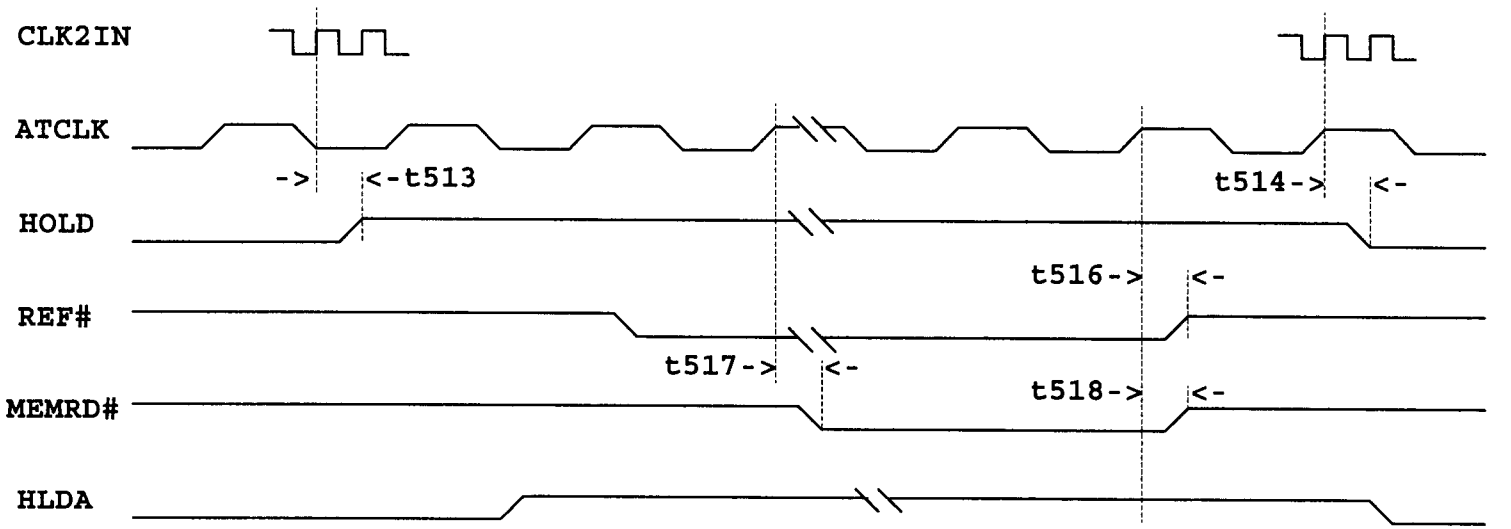
KBDCS# VALID AND INVALID DELAY

10.30 ATBUS Timings



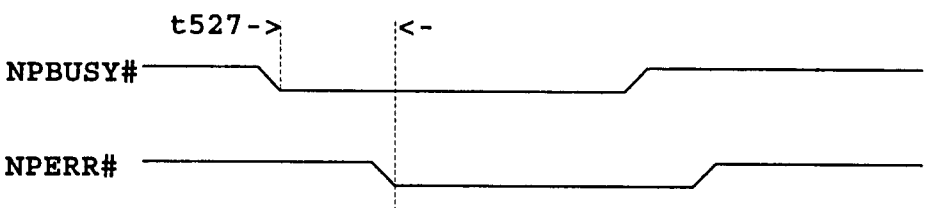
ATBUS TIMINGS

10.31 ATBUS Hold Timings



ATBUS HOLD TIMING

10.32 NPBUSY, FERR# Timing



NPBUSY, FERR# TIMING

Appendix A - 82C463 Compatibility Summary

A.1 Introduction

The purpose of testing the OPTi 82C463 is to assure compatibility with available software and hardware products under DOS, OS/2, UNIX and LAN environments. To assure compatibility, we have set up rigorous test procedures for each software and hardware product. These tests concentrate on specific areas where potential problems are most likely to occur. Software test areas would include the installation process, file management, memory management, input/output and functionality. Hardware test areas include hardware settings, software (driver) installation, functionality and reliability. Other forms of testing we perform include stress testing, volume testing and regression testing. The products that pass all of these tests are added into the TEST RESULTS section and are listed on the Compatibility Certification sheet. The third party software and hardware products that are not available at test time will be tested and certified later when they become available. This is just a preliminary test report. As further testing is completed, a final test report will be issued.

OPTi Test Labs
January 14, 1993

A.2 Test Platform Specifications

DOS/Windows Platform

Platform Name:	OPTi 486 Notebook
ROM BIOS:	Phoenix
Processor:	Intel 486DX
CPU Speed:	25MHz
Chip Set:	OPTi 82C463 (5V)
External Cache:	0K
System Architecture:	ISA
Motherboard Mfg/Rev:	OPTi 486NB-Single Chip-6A1B1
Video Adaptor:	VGA
Hard Drive:	SCSI, ESDI, IDE, MFM
Hard Drive Controller:	SCSI, ESDI, IDE, MFM
Floppy Drive:	1.44MB 3.5" & 1.2MB 5.25"
Base Memory:	640KB
Extended Memory:	7168KB
Operating System:	MS-DOS v3.3, v5.0

IBM OS/2 Platform

Platform Name:	OPTi 486 Notebook
ROM BIOS:	Phoenix
Processor:	Intel 486DX
CPU Speed:	25MHz
Chip Set:	OPTi 82C463 (5V)
External Cache:	0K
System Architecture:	ISA
Motherboard Mfg/Rev:	OPTi 486NB-Single Chip-6A1B1
Video Adaptor:	VGA
Hard Drive:	SCSI, IDE
Hard Drive Controller:	SCSI, IDE
Floppy Drive:	1.44MB 3.5" & 1.2MB 5.25"
Base Memory:	640KB
Extended Memory:	7168KB
Operating System:	IBM OS/2 v1.3, v2.0

LAN Platform	
Platform Name:	OPTi 486 Notebook
ROM BIOS:	Phoenix
Processor:	Intel 486DX
CPU Speed:	25MHz
Chip Set:	OPTi 82C463 (5V)
External Cache:	0K
System Architecture:	ISA
Motherboard Mfg/Rev:	OPTi 486NB-Single Chip-6A1B1
Video Adaptor:	VGA
Hard Drive:	SCSI, IDE
Hard Drive Controller:	SCSI, IDE
Floppy Drive:	1.44MB 3.5" & 1.2MB 5.25"
Base Memory:	640KB
Extended Memory:	7168KB
Operating System:	DOS 5.0 / Novell NetWare v3.11

A.3 Test Plan

MS-DOS

INSTALLATION (subject installed where available)

1. Full basic installation of DOS system
2. Software installation - DOS applications
3. Hardware installation - video display, mouse, printer

OPERATING SYSTEM TEST

1. File management system
2. Memory management - upper memory, XMS memory management
3. Internal and external command execution
4. Device Driver installation and support
5. Editor - edlin, edit
6. Dosshell - for version 5.0
7. Output - print command, print-screen
8. DOS application test - refer to APPLICATION TEST section

MS-WINDOWS

INSTALLATION (subject installed where available)

1. Full installation of MS-Windows program
2. Software installation - DOS applications, Windows applications
3. Hardware installation - video display, mouse, printer

OPERATING SYSTEM TEST

1. Help/Tutorial
2. File management - new icon/group, delete icon/group, move, open, properties, run
3. Desktop management - restore, move, size, minimize, maximize, close, switch to
4. Main group system programs - file manager, control panel, print manager, windows setup, clipboard viewer, PIF editor, MS-DOS prompt
5. Accessories group system programs - write, paintbrush, terminal, notepad, recorder, cardfile, calendar, calculator, clock
6. Games group - solitaire, reversi, minesweeper
7. Startup group
8. Output
9. Windows application test - refer to APPLICATION TEST section

IBM OS/2

INSTALLATION (subject installed where available)

1. Full basic installation of OS/2 system
2. Software installation - install OS/2 applications, DOS/Windows application migration
3. Hardware installation - video display, mouse, printer

OPERATING SYSTEM TEST

1. Help/Tutorial
2. File management - create new, open existing, close current, copy, delete
3. Desktop management - arrange icons, minimize, maximize, move, close and sizing windows, and shut down system
4. Multitasking - multi-task between multiple OS/2 Windows and OS/2 Full Screen
5. System programs - file manager, calendar, notepad, system editor
6. Import DOS & Windows applications
7. Output
8. OS/2 application test - refer to APPLICATION TEST section

LAN

INSTALLATION (subject installed where available)

1. Full basic installation of LAN system
2. Software installation - DOS applications
3. Hardware installation - printers

INITIALIZATION

1. Load IPX or netbios TSR
2. Load Net5
3. Login - supervisor, superuser, network administrator

NETWORK FUNCTIONALITY & MANIPULATION

1. Send messages to and from server
2. Test and verify file sharing and record locking
3. Alter users access to files and directories

INPUT/OUTPUT

1. Print files to shared or local printers
2. Copy files to shared and local directories, local floppy disk drives

APPLICATION TEST (subject tested where supported)

WORD PROCESSOR

1. Installation - basic or automatic installation; custom installation with all options
2. Help/Tutorial - run help option indexing sample topics; run tutorial program
3. File Management - create new, open existing, close current, save document, import/export
4. Editing Functions - undo, copy, delete, move, search/replace
5. Document Format - font, size, attributes, spacing, alignment, zoom, tabs, page setup
6. Tools & Utilities - spell check, thesaurus, dictionary, grammar, shell to DOS, security protection
7. Macro - create sample macro routine and execute
8. Output - printer setup, print preview, print document
9. Special Added Features - Graphics mode support, style sheet/template options

SPREADSHEET

1. Installation - basic or automatic installation; custom installation with all options
2. Help/Tutorial - run help option indexing sample topics; run tutorial program
3. File Management - create new, open existing, close current, save document, import/export
4. Editing Functions - undo, copy, cut, paste, move, search/replace, insert/delete rows/columns
5. Document Format - font, size, attributes, pattern, alignment, row/column resizing, page setup
6. Tools & Utilities - formula handling, sorting, calculate, math functions, split screen, protection security, charting/graphing
7. Macro - create sample macro routine and execute
8. Output - printer setup, print preview, print document

DATABASE

1. Installation - basic or automatic installation; custom installation with all options
2. Help/Tutorial - run help option indexing sample topics; run tutorial program
3. File Management - create new, open existing, close current, save document, import/export
4. Editing Functions - copy, insert, delete, append, replace, mark, find
5. Document Format - page format, fonts, text attributes(bold, italics, underline), field descriptions (character, number, logic, date, memo), justification
6. Tools & Utilities - sort, title page generator, report style, graphics capabilities
7. Macro - create sample macro and execute
8. Output - printer setup, print preview, print sample file

GRAPHICS

1. Installation - basic or automatic installation; custom installation with all options
2. Help/Tutorial - run help option indexing sample topics; run tutorial program
3. File Management - create new, open existing, close current, save document, import/export
4. Editing Functions - undo, copy, cut, paste, move, rotate, flip, blend, mirror
5. Document Format - font, size, attributes, spacing, alignment, magnification(zoom), page setup, rulers, grid
6. Tools & Utilities - toolbox, brush size, line type, arrow type, shapes, curves, pencil, erase, color, patterns
7. Macro - create sample macro and execute
8. Output - printer setup, print preview, print sample drawing

DESKTOP PUBLISHING

1. Installation - full installation with all options including applicable drivers
2. Help/Tutorial - run help option indexing sample topics; run tutorial program
3. File Management - create new, open, close, save, merge, import/export
4. Editing Functions - undo, copy, cut, paste, clear, insert, select all, group, rotate, wrap
5. Document Format - font, size, attributes, spacing, alignment, magnification(zoom), page setup, tab, ruler, template, grid
6. Tools & Utilities - toolbox, line type, image control, search & replace, color, pattern, dictionary, spell check, thesaurus,symbols(math)
7. Macro - create sample macro and execute
8. Output - printer setup, print preview, print sample document

CAD

1. Installation - full installation with all options including applicable drivers
2. Help/Tutorial - run help option indexing sample topics; run tutorial program
3. File Management - create new, open existing, close current, save, delete, copy, import/export
4. Editing Functions - undo, copy, cut, paste, clear, hide/show,
5. Document Format - font, size, attributes, ruler(polar coordinates), patterns, alignment, page setup, magnification(zoom), grid,
6. Tools & Utilities - toolbox, arcs, polygons, circle, brush size, trim, mirror, scaling, rotating, 3D-effects
7. Macro - create sample macro and execute
8. Output - printer setup, print preview, print sample document

UTILITIES

1. Installation - full installation with all options including applicable drivers
2. Help/Tutorial - run help option indexing sample topics; run tutorial program
3. Utility options - test each utility functions
4. Output - printer setup, print results

A.4 Test Matrix

RPT #	WINDOWS APPLICATIONS	VENDOR	DATE	STATUS
1	Windows v3.1	Microsoft	1/11/93	Pass
2	Word for Windows v2.0	Microsoft	1/11/93	Pass
3	Excel for Windows v3.0	Microsoft	1/11/93	Pass
4	Pagemaker v4.0	Aldus	1/11/93	Pass
5	Windows Draw v3.0	Micrografix	1/11/93	Pass
6	PC Tools Deluxe v7.1	Central Point	1/11/93	Pass
7	PowerPoint Presentation v2.0	Microsoft	1/11/93	Pass
8	Ami Pro v2.0	Lotus Development	1/11/93	Pass
9	Excel for Windows v4.0	Microsoft	1/11/93	Pass
10	Visual Basic v1.0	Microsoft	1/11/93	Pass

RPT #	DOS APPLICATIONS	VENDOR	DATE	STATUS
12	AutoCAD v11	Autodesk	1/12/93	Pass
13	Paradox v3.5	Borland	1/11/93	Pass
14	Word Perfect v5.1	Word Perfect	1/11/93	Pass
15	Harvard Graphics v3.0	Software Publishing	1/11/93	Pass
16	Lotus 1-2-3 v3.1	Lotus Development	1/11/93	Pass

RPT #	OPERATING SYSTEMS	VENDOR	DATE	STATUS
18	OS/2 v1.3	IBM	1/12/93	Pass
19	OS/2 v2.0	IBM	1/12/93	Pass
20	Novell Netware v2.2	Novell	1/14/93	Pass
21	Novell Netware v3.11	Novell	1/13/93	Pass

RPT #	CONTROLLERS	VENDOR	DATE	STATUS
30	IDE & floppy controller	Generic	1/8/93	Pass
35	U12F ESDI	UltraStor	1/11/93	Pass

RPT #	HARD DRIVES	VENDOR	DATE	STATUS
39	Maxtor LXT213A	Maxtor	1/14/93	Pass
40	MiniScribe MS-8051A IDE	MiniScribe	1/14/93	Pass
41	Teac SD-340 IDE	Teac	1/14/93	Pass
44	Micropolis 1664-7 ESDI	Micropolis	1/14/93	Pass

RPT #	GRAPHICS ADAPTER	VENDOR	DATE	STATUS
57	ATI VGA Wonder+	ATI	1/14/93	Pass
58	Headland VGA 1024i	Headland	1/14/93	Pass
59	Orchid ProDesigner II	Orchid	1/14/93	Pass
60	Video 7 V-RAM VGA	Video Seven	1/14/93	Pass
61	Trident VGA	Trident	1/14/93	Pass
62	Orchid Fahrenheit 1280 VGA	Orchid	1/14/93	Pass

A.4 Test Matrix (con't)

RPT #	INPUT DEVICES	VENDOR	DATE	STATUS
65	MS-Serial PS/2 Mouse	Microsoft	1/12/93	**Pass**
66	Logitech Serial Mouse	Logitech	1/12/93	**Pass**

RPT #	PRINTERS	VENDOR	DATE	STATUS
67	HP-Laserjet Series II	Hewlett Packard	1/12/93	**Pass**

RPT #	SOUND BLASTER	VENDOR	DATE	STATUS
68	Sound Blaster Pro	Creative Labs	1/12/93	**Pass**

RPT #	LAN ADAPTERS	VENDOR	DATE	STATUS
70	Ethernet 10BaseT CN600E	CNet	1/12/93	**Pass**
71	Ethernet 10BaseT CN800E	CNet	1/12/93	**Pass**
72	Ethernet NE1000	Novell	1/12/93	**Pass**
73	Ethernet NE2000	Novell	1/12/93	**Pass**
74	Ethernet DE-200	DLink	1/12/93	**Pass**
75	Ethernet 3C503	3Com	1/12/93	**Pass**

(End of compatability test report.)

HeadQuarters, USA

California
OPTi, Inc.
2525 Walsh Ave
Santa Clara, CA 95051
tel: (408)980-8178 x216
fax: (408)980-8860

Sales Offices

OPTi, Inc.
Territory: ***Taiwan***
9F, No 303, Sec 4, Hsin Yih Road,
Taipei, Taiwan, ROC
tel: 011-886-2-325-8520
fax: 011-886-2-325-6520

Representatives

Western Region

Brooks Technical Group
Territory: ***N. CA, N. NV***
883 N. Shoreline Blvd.
Mountain View, CA 94043
tel: 415-960-3880
fax: 415-960-3615

Jones & McGeoy Sales
Territory: ***CA,Orange County, SFV***
5100 Campus Dr. #300
Newport Beach, CA 92660
tel: 714-724-8080
fax: 714-724-8090

Electronic Component Sales
Territory: ***Oregon***
3879 South West Hall Blvd.
Beaverton, OR 97075
tel: 503-245-2342
fax: 503-520-0767

Electronic Component Sales
Territory: ***Washington, BC, Canada***
9311 S.E. 36th Street
Mercer Island, WA 98040-3795
tel: 206-232-9301
fax: 206-232-1095

Excel USA
Territory: ***San Diego***
6885 Flanders Dr.
San Diego, CA 92121
tel: 619-587-0545
fax: 619-587-1380

Excel USA
Territory: ***Arizona, New Mexico***
1515 W. University Dr., #103
Tempe, AZ 85281
tel: 602-829-8820
fax: 602-967-2658

Excel USA
Territory: ***Colorado, Utah***
384 Inverness Dr. South, #105
Englewood, CO 80112
tel: 303-649-1800
fax: 303-649-1818

Central Region

OPTi, Inc.
Territory: ***Texas***
2525 Walsh Ave
Santa Clara, CA 95051
tel: (408)980-8178 x226
fax: (408)980-8860

Concord Component Reps
Territory: ***Alabama, MS***
190 Line Quarry Rd. Ste 102
Madison, AL 35758
tel: 205-772-8883
fax: 205-772-8262

Jay Marketing
Territory: ***Michigan***
763 Wing St.
Plymouth, MI 48170
tel: 313-459-1200
fax: 313-459-1697

Lyons Corp.
Territory: ***OH (Dayton), W.PA***
4615 W. Streetsboro
Dayton, OH 45414
tel: 513-278-0714
fax: 513-278-3609

Lyons Corp.
Territory: ***OH (Richfield),W.PA***
Richfield, OH 44286
tel: 216-659-9224
fax: 216-659-9227

Lyons Corp.
Territory: ***OH (Cleveland),W.PA***
248 N. State Street
Westerville, OH 43081
tel: 614-895-1447
fax: Same

LTD Technologies, Inc.
Territory: ***Illinois, WI***
810 Arlington Heights Rd.
Itasca, IL 60143-1411
tel: 708-773-2900
fax: 708-773-0358

LTD Technologies, Inc.
Territory: ***Wisconsin***
10855 W. Potter Rd.
Milwaukee, WI 53226
tel: 414-774-1000
fax: 414-774-0593

Stan Clothier Company
Territory: ***Minnesota***
9600 W. 76th Street, Ste. A
Eden Prairie, MN 55344
tel: 612-944-3456
fax: 612-944-6904

Eastern Region

OPTi, Inc.
Territory: ***Eastern Canada***
2525 Walsh Ave
Santa Clara, CA 95051
tel: (408)980-8178 x346
fax: (408)980-8860

EIR, Inc.
Territory: ***Florida***
1057 Mainland Center Commons
Maitland, FL 32794-5057
tel: 407-660-9600
fax: 407-660-9091

S-J Associates, Inc.
Territory: ***New York***
265 Sunrise Highway
Rockville Centre, NY 11570
tel: 516-536-4242
fax: 516-536-9638

S-J Associates, Inc.
Territory: ***Chesapeake VA***
900 S. Washington St., Suite B2
Falls Church, VA 22046
tel: 703-533-2233
fax: 703-533-2236

S-J Associates, Inc.
Territory: ***New Jersey, E.PA***
131-D Gaither Dr.
Mt. Laurel, NJ 08054
tel: 609-866-1234
fax: 609-866-8627

Concord Component Reps
Territory: ***Georgia, NC, SC***
6048 Tracy Valley Drive
Norcross, GA 30093
tel: 404-416-9597
fax: 404-441-0790

Concord Component Reps
Territory: ***N. Carolina, SC***
3509 Morning Side Dr.
Raleigh, NC 27607-3024
tel: 919-676-3900
fax: 919-676-3070

International Regions

ASEC International Corp.
Territory: ***Taiwan***
7F No. 344-1, Min-Sheng E. Road
Taipei, Taiwan ROC
tel: + 886-2-505-7025

Braemac Pty. Ltd.
Territory: ***Australia***
Unit 6, 111 Moore Street, Leichhardt
Sydney, 2040 Australia
tel: + 61-2-564-1211
fax: + 61-2-564-2789

Consystem SRI
Territory: ***Italy***
Via Gramsci, 156 Paderno Dugnano,
(MI)
Italy, 20037
tel: + 39 (2) 99041977
fax: + 39 (2) 99041981

Dia Semicon Systems, Inc.
Territory: ***Japan***
Flowerhill-Shinmachi,
1-23-9 Hsinmachi Setagaya-Ku
Tokyo 154, Japan
tel: + 81-3-3439-2700
fax: + 81-3-3439-2701

Dynax Electronics, Ltd.
Territory: ***Hong Kong***
Unit 1, 21/F Star Centre
443-451 Castle Peak Road
Kwai Chung, N.T. Hong Kong
tel: + 85 (2) 481-0223
tel: + 85 (2) 796-5913
fax: + 85 (2) 481-0826

FM Korea
Territory: ***Korea***
3rd Fl, Elim Bldg, 203-13
Yangjae-dong, Seocho-ku,
Seoul, Korea. Post # 137-130
tel: 822-575-9720
fax: 822-575-9732

Manhattan Skyline, Ltd.
Territory: ***United Kingdom***
Unit 1, The Switchback, Gardener Rd.
Maidenhead, Berkshire UK SLC7RJ
tel: + 44 (628) 75851
fax: + 44 (628) 782812

Micro Summit
Territory: ***Japan***
Premier K1, Bldg 4F,
1 Kanda, Mikura-Cho, Chiyoda-Ku
Tokyo 101, Japan
tel: + 81-3-3258-5531
fax: + 81-3-3258-0433

Tekelec Airtronic ,France
Territory: ***France***
5 Rue Carle Vernet, BP.2
92135 Sevres, Cedex, France
tel: + 33 (1) 46232407
fax: + 33 (1) 45072191

Uniao Digital
Territory: ***Brazil***
Rua Georgia, 69-Brooklin Novo
04559-010-Sao Paulo-Brazil
tel: + 55-11-533-4121
fax: + 55-11-533-6780

Westech Electronics Pte. Ltd.
Territory: ***Singapore***
12 Lorong Bakar Batu, #05-07,
Kolam Ayer Industrial Park
Singapore, 1334
tel: + 65-743-6355
fax: + 65-746-1396

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